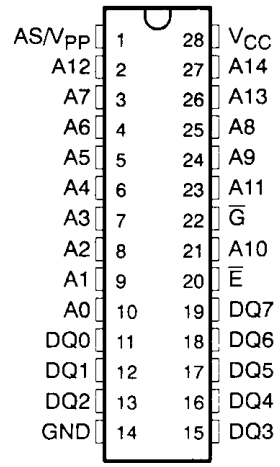
- **Organization . . . 32K × 8**
- **Single 5-V Power Supply**
- **Intergrated Address Latch**
- **Max Access/Min Cycle Time (V_{CC} ± 5%)**

TMS87C257-150	**150 ns**
TMS87C257-1	**170 ns**
TMS87C257-2	**200 ns**
TMS87C257	**250 ns**

- **Power-Saving CMOS Technology**
- **Very High-Speed SNAP! Pulse Programming**
- **3-State Output Buffers**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **— Active . . . 263 mW Worst Case**
  - **— Standby . . . 1.4 mW Worst Case (CMOS Input Levels)**

J Package
(Top View)



PIN NOMENCLATURE	
A0-A14	Address Inputs
$\overline{E}$	Chip Enable/Powerdown
$\overline{G}$	Output Enable
GND	Ground
NC	No Internal Connection
NU	Make No External Connection
DQ0-DQ7	Inputs (programming)/Outputs
V_{CC}	5-V Power Supply
AS/V_{PP}	Address Strobe/13-V Programming Power Supply

description

The TMS87C257 series are 262 144-bit, ultra-violet-light erasable, electrically programmable read-only memories.

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs(including program data inputs) can be driven by Series 74 TTL circuits without the use of external pullup resistors. Each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS87C257 incorporates internal address latches on address inputs A0-A7. The internal address latch allows address and data pins to be tied directly to the processor's multiplexed address/data pins which can simplify design, reduce chip connect, and lower the cost of multiplexed bus systems.

The TMS87C257 is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS87C257 is characterized for operation from – 40°C to 85°C (E suffix).

These EPROMs operate from a single 5-V supply (in the read mode), thus are ideal for use in microprocessor-based systems. One other 13 V supply is needed for programming . All programming signals are TTL level. These devices are programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13 V and a V_{CC} of 6.5 V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

operation

There are seven modes of operation listed in the following table. The read mode requires a single 5-V supply. AS/V_{PP} during programming requires 13 V for SNAP! Pulse and 12 V on A9 for signature mode.

FUNCTION	MODE							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
$\overline{E}$	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
$\overline{G}$	V_{IL}	V_{IH}	X†	V_{IH}	V_{IL}	X	V_{IL}	
AS/V_{PP}	V_{IL}§	X	X	V_{PP}	V_{PP}	V_{PP}	V_{IH}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_H‡	V_H‡
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0-DQ7	Data Out	HI-Z	HI-Z	Data In	Data Out	HI-Z	CODE	
							MFG	DEVICE
							97	C2

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.
§ V_{IL} latches the address inputs A0-A7, V_{IH} unlatches those inputs.

read/output disable

When the outputs of two or more TMS87C257s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to the $\overline{G}$ pin while the device is powered up ($\overline{E}$ is low). Output data is accessed at pins DQ0 through DQ7.

latchup immunity

Latchup immunity on the TMS87C257 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the EPROM is interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

For more information see application report SMLA001, *"Design Considerations; Latchup Immunity of the HVCMOS EPROM Family"*, available through TI Sales Offices.

power down

Active I_{CC} supply current can be reduced from 30 mA to 250 μA (CMOS-level inputs) by applying a high-level (CMOS) signal to the $\overline{E}$ pin. In this mode all outputs are in the high-impedance state, independent of $\overline{G}$. Data and address inputs are at static CMOS levels.

erasure

Before programming, the TMS87C257 EPROM is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). EPROM erasure before programming is necessary to assure that all bits are in the logic high state. Logic lows are programmed into the desired locations. A programmed logic low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A typical 12-mW/cm^2, filterless UV lamp will erase the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS87C257, the window should be covered with an opaque label. After erasure (all bits in logic high state), logic lows are programmed into the desired locations. A programmed zero low can be erased only by ultraviolet light.

SNAP! Pulse programming

The 256K latched CMOS EPROM is programmed using the TI SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1, which can reduce time to a nominal of four seconds. Actual programming time will vary as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, $\overline{E}$ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (μs) followed by a byte verification to determine when the addressed byte has been successfully programmed. Up to 10 (ten) 100-μs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when AS/V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{G}$ = V_{IH}, and $\overline{E}$ = V_{IL}. During the programming mode, the address latch becomes effectively transparent. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V.

program inhibit

Programming may be inhibited by maintaining a high level input on the $\overline{E}$ pin.

program verify

Programmed bits may be verified with AS/V_{PP} = 13 V when $\overline{G}$ = V_{IL} and $\overline{E}$ = V_{IH}.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 is forced to 12 V ± 0.5 V. Two identifier bytes are accessed by A0; i.e., A0 = V_{IL} accesses the manufacturer code, which is output on DQ0-DQ7; A0 = V_{IH} accesses the device code, which is output on DQ0-DQ7. All other addresses must be held at V_{IL}. Each byte possesses odd parity on bit DQ7. The manufacturer code for these devices is 97, and the device code is C2.

memory address lines

Fifteen memory address lines (A0-A14) are provided on the device and are used in conjunction with $\overline{G}$ and $\overline{E}$ to select one of 32 768 eight bit locations in the memory array. Addresses A0 through A7 are latched on the negative edge of the address strobe signal.

address strobe line

The address strobe (AS) input is multiplexed with V_{PP} on pin 1. The negative edge of AS latches the low order address lines (A0-A7) to demultiplex the address/data bus while the positive edge of AS unlatches these address lines.

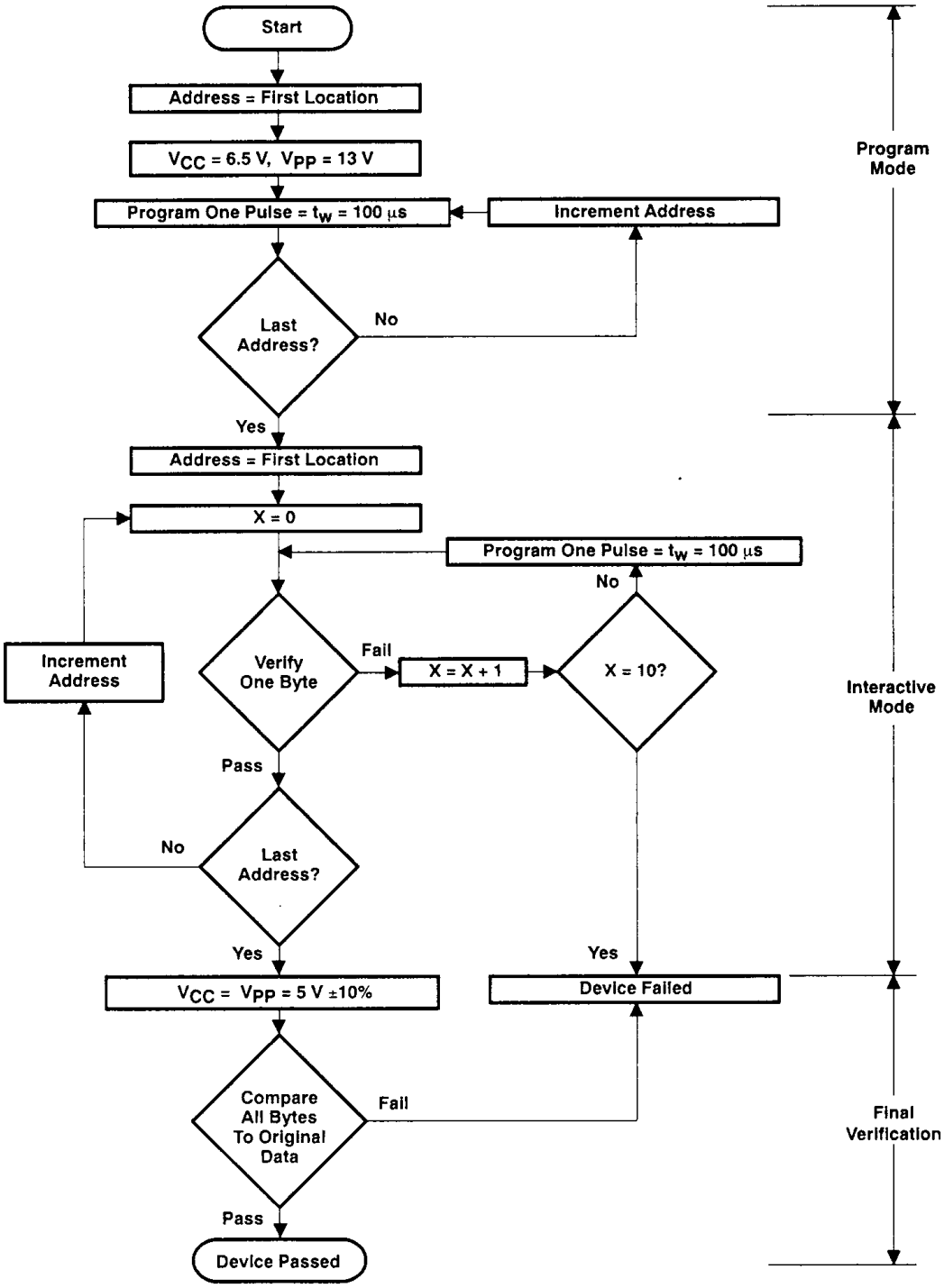
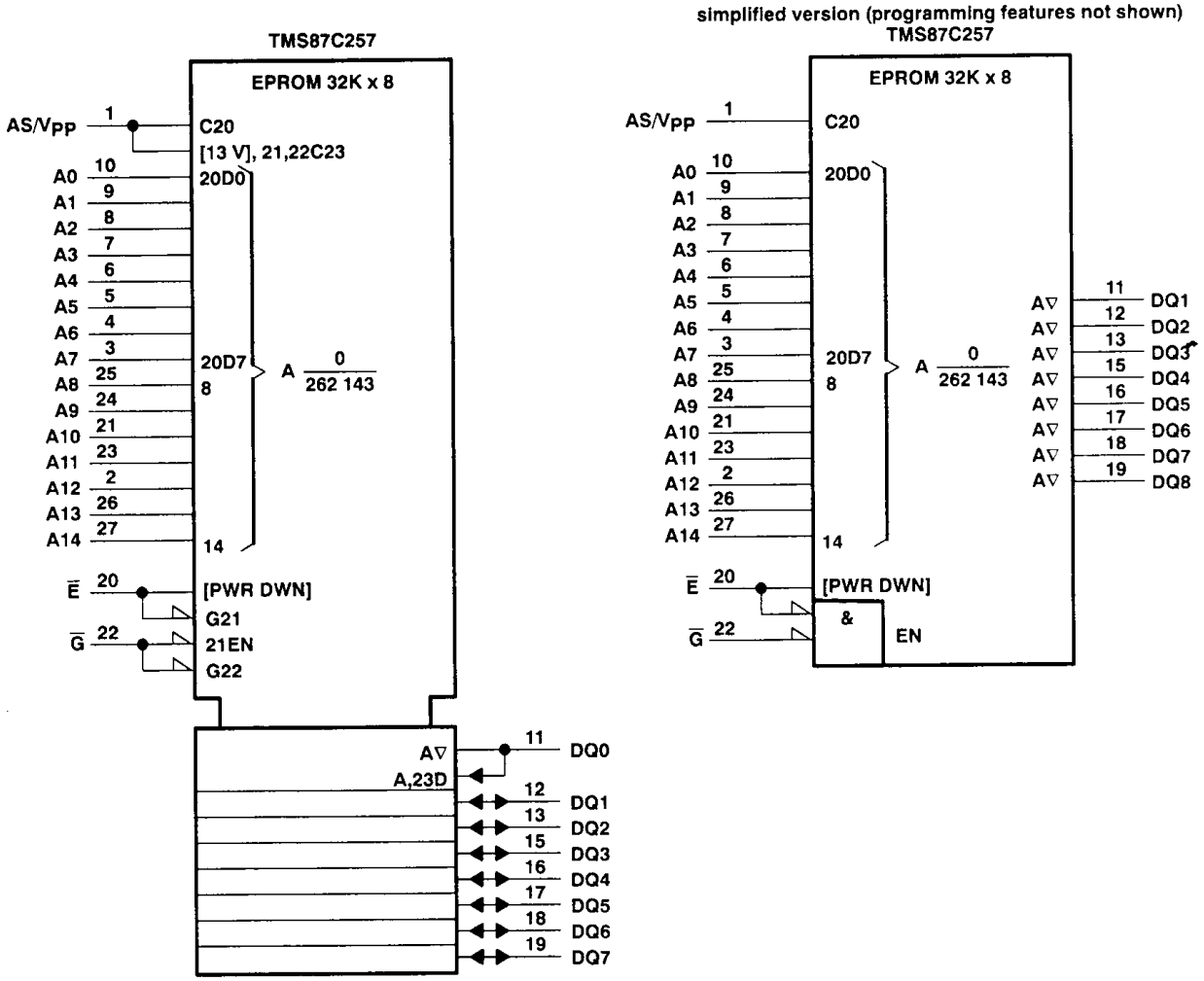


Figure 1. SNAP! Pulse Programming Flowchart

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} (see Note 1) . . . . . – 0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . – 0.6 V to 14 V
Input voltage range (see Note 1): All inputs except A9 . . . . . – 0.6 V to 6.5 V
A9 . . . . . – 0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . – 0.6 V to V_{CC} + 1 V
Operating free-air temperature range ('87C257-_ _JE . . . . . – 40° C to 85°C
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

			TMS87C257-150 TMS87C257-1 TMS87C257-2 TMS87C257			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage	Read mode (see Note 2)	4.75	5	5.25	V
		SNAP! Pulse programming algorithm	6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode (see Note 3)	VCC – 0.6		VCC + 0.6	V
		SNAP! Pulse programming algorithm	12.75	13	13.25	
V_{IH}	High-level input voltage (CMOS)		VCC × 0.7		VCC + 1	V
V_{IL}	Low-level input voltage (CMOS)		– 0.5		0.8	V
T_A	Operating free-air temperature		– 40		85	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$.

electrical characteristics over full ranges of operating conditions

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = – 2.5 mA	3.5			V
			I_{OH} = – 20 μA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 2.1 mA			0.4	V
			I_{OL} = 20 μA			0.1	
I_I	Input current (leakage)		V_I = 0 to 5.5 V			±1	μA
I_O	Output current (leakage)		V_O = 0 to V_{CC}			±1	μA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5 V		1	10	μA
I_{PP2}	V_{PP} supply current (during program pulse)		V_{PP} = 13 V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	CMOS-input level	V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	250	μA
I_{CC2}	V_{CC} supply current (active)		V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		15	30	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance §	V_I = 0, f = 1 MHz		6	10	pF
C_O	Output capacitance	V_O = 0, f = 1 MHz		10	14	pF

†Typical values are at T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.
§ AS/V_{PP} is not included in input capacitance.

switching characteristics over full ranges of recommended operating conditions (see Notes 4 and 5)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 & 5)	'87C257-150		'87C257-1		'87C257-2		'87C257		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL Load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns		150		170		200		250	ns
$t_{a(E)}$	Access time from chip enable			150		170		200		250	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			75		75		75		100	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	60	0	60	0	60	0	60	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first†		0		0		0		0		ns
$t_{su(AS)}$	Address to AS/V_{PP} fall		20		20		20		20		ns
$t_{w(AS)}$	Address strobe pulse width		90		90		90		90		ns
$t_{h(AS)}$	Address hold from AS/V_{PP} fall		30		30		30		30		ns

†Value calculated from 0.5 V delta to measured level. This parameter is only sampled and not 100% tested.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V, T_A = 25°C (see Note 4)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0		130	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150	ns

NOTES: 4. For all switching characteristics the input pulse levels are 0.4 V to V_{CC} × 0.7 V. Timing measurements are made at 3 V for logic high and 0.8 V for logic low. (reference AC Testing Wave Form)

5. Common test conditions apply for the t_{dis} except during programming.

recommended timing requirements for programming: V_{CC} = 6.5 V and V_{PP} = 13 V, T_A = 25°C (see Note 4)

		MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Program pulse duration	95	100	105	µs
$t_{su(A)}$	Address setup time	2			µs
$t_{su(G)}$	$\overline{G}$ setup time	2			µs
$t_{su(E)}$	$\overline{E}$ setup time	2			µs
$t_{su(D)}$	Data setup time	2			µs
$t_{su(VPP)}$	V_{PP} setup time	2			µs
$t_{su(VCC)}$	V_{CC} setup time	2			µs
$t_{h(A)}$	Address hold time	0			µs
$t_{h(D)}$	Data hold time	2			µs

NOTE 4: For all switching characteristics the input pulse levels are 0.4 V to V_{CC} × 0.7 V. Timing measurements are made at 3 V for logic high and 0.8 V for logic low). (reference AC Testing Waveform)

PARAMETER MEASUREMENT INFORMATION

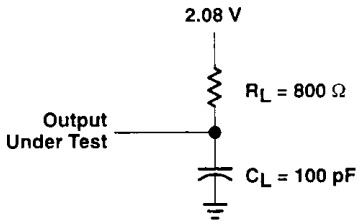
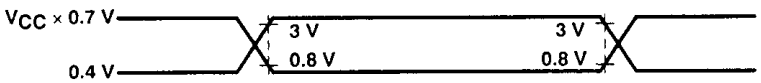


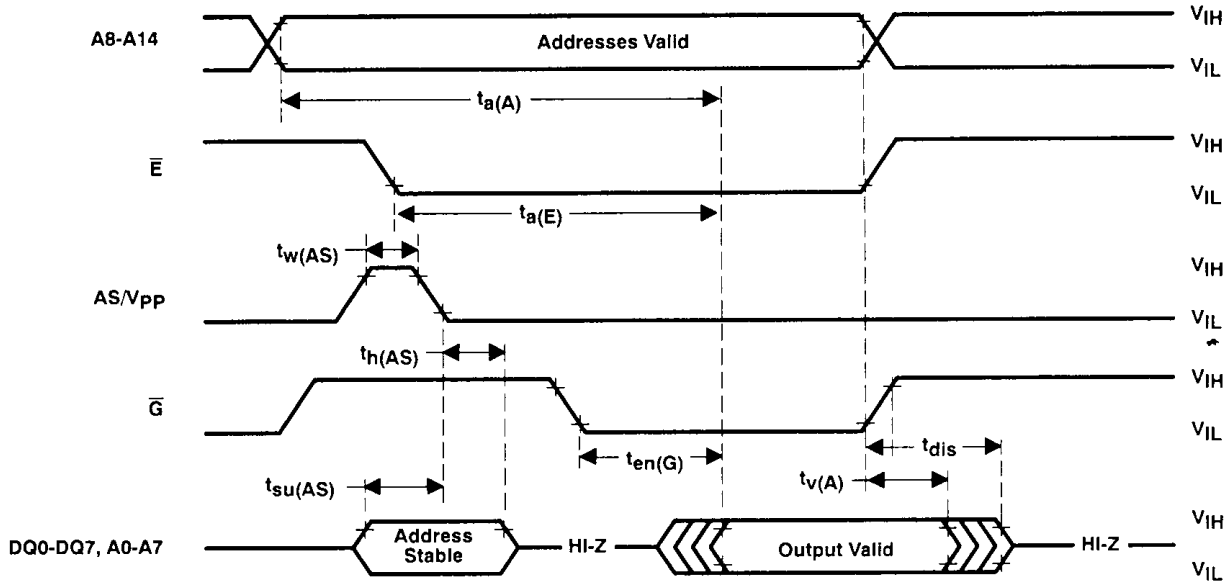
Figure 2. AC Testing Output Load Circuit

AC testing input/output wave forms

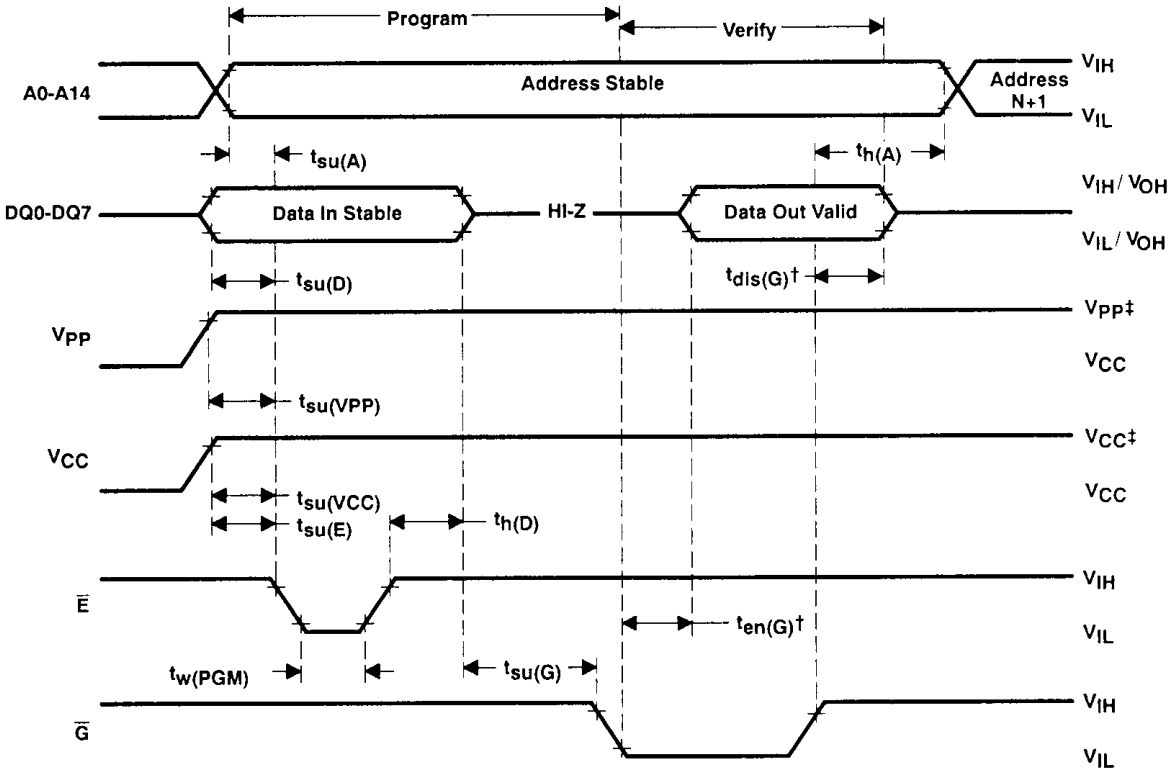


A.C. testing inputs are driven at V_{CC} × 0.7 V for logic high and 0.4 V for logic low. Timing measurements are made at 3 V for logic high and 0.8 V for logic low for both inputs and outputs.

read cycle timing



program cycle timing (SNAP! Pulse programming)



† $t_{dis(G)}$ and $t_{en(G)}$ are characteristics of the device but must be accommodated by the programmer.
‡ 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming.