REF Schematic for RK3568

Main Functions Introduction

1)PMIC: RK809-5+DiscretePower
2)RAM: DDR4 2x16Bit------------------Default
Option:LPDDR4/4x 1X32bit(200ball)
Option:DDR3 4x16bit
Option:DDR3 4x16bit+2x16bit ECC
Option:DDR4 2x16bit+1x16bit ECC
Option:LPDDR3 1x32bit(178ball)
Option:DDR4 4x16bit
3)ROM: eMMC--------------------------Default
Option:Nand Flash
Option:SPI Flash
4)Support:1 x Micro SD Card3.0
5)Support:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1 + 1 x SATA3.0 Port2 ----------Default
Option:1 x USB3.0 OTG0 + 1 x USB3.0 HOST1 + 1 x 1Lane PCIe2.0(RC Mode)
Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
Option:1 x USB3.0 OTG0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x SATA3.0 Port2
Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB3.0 HOST1 + 1 x 1Lane PCIe2.0(RC Mode)
Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x SATA3.0 Port2
Option:1 x USB2.0 OTG0 + 1 x SATA3.0 Port0 + 1 x USB2.0 HOST1 + 1 x SATA3.0 Port1 + 1 x 1Lane PCIe2.0(RC Mode)
6)Support:1 x USB2.0 HOST2+ 1 x USB2.0 HOST3 -- ------Default
7)Support:4G module Via MiniPCIe2.0 Slot With PCIE2.0 and USB2.0 HOST3 function ------Option
8)Support:2 x 1Lane PCIe3.0 Connector (RC Mode) ------Default
Option:1 x 2Lanes PCIe3.0 Connector (RC Mode)
Option:1 x 2Lanes PCIe3.0 Connector (EP Mode)
9)Support:1 x HDMI2.0 TX
10)Support:1 x LCM MIPI DSI TX0 ----------Default
Option:1 x LCM MIPI DSI TX1
Option:1 x LCM LVDS TX
Option:1 x LCM Dual MIPI DSI TX
Option:1 x LCM eDP TX
11)Support:1 x VGA OUT ----------Default
12)Support:1 x 4Lanes Camera MIPI CSI RX ----------Default
Option:2 x 2Lanes Camera MIPI CSI RX
Option:1 x HDMI1.4 RX(HDMI to MIPI CSI)
13)Support:a/b/g/n/ac 2X2 SDIO WIFI5+BT5.0+PCM --------Default
Option:a/b/g/n/ac 1X1 SDIO WIFI+BT+PCM
Option:a/b/g/n/ac/ax 2X2 PCIe WIFI6+BT5.0+PCM
14)Support:1 x 10/100/1000M Ethernet(RGMII1_M1) -------Default
Option:1 x 10/100/1000M Ethernet(RGMII0) or 1 x 10/100M Ethernet(RMII0)
Option:1 x 10/100/1000M PCIe Ethernet Card or 2 x 10/100/1000 Ethernet(QSGMII) or 1 x 10/100/1000 Ethernet(SGMII)
15)Support:1 x Headphone output ----------Default
16)Support:1 x ECM MIC + 1 x Speaker out -------------Default
Option:4 x MEMS MIC + 1 x Speaker out + Loopback or 2 x MEMS MIC + 1 x Speaker out + Loopback
Option:4 x MEMS MIC + 2 x Speaker out + Loopback
17)Support:1 x IR Receiver ----------Default
18)Support:Array Key(MENU,VOL+,VOL-,ESC),Reset,Power on/off Key
19)Support:3 x UART + 1 x RS485 + 1 x CAN FD(Option)
20)Support:Debug UART and ARM JTAG

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Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	1 of 72

Table of Content

Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-02-04	Zhangdz	1:Revision preliminary version	
V1.1	2021-06-11	Zhangdz	1:Change content Please Refer to: RK3568_AIoT_REF_SCH_V11_20210611_Modify_Notes	

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Project:	RK3568_AIoT_REF_SCH				
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Date:	Wednesday, June 16, 2021			Rev:	V1.1
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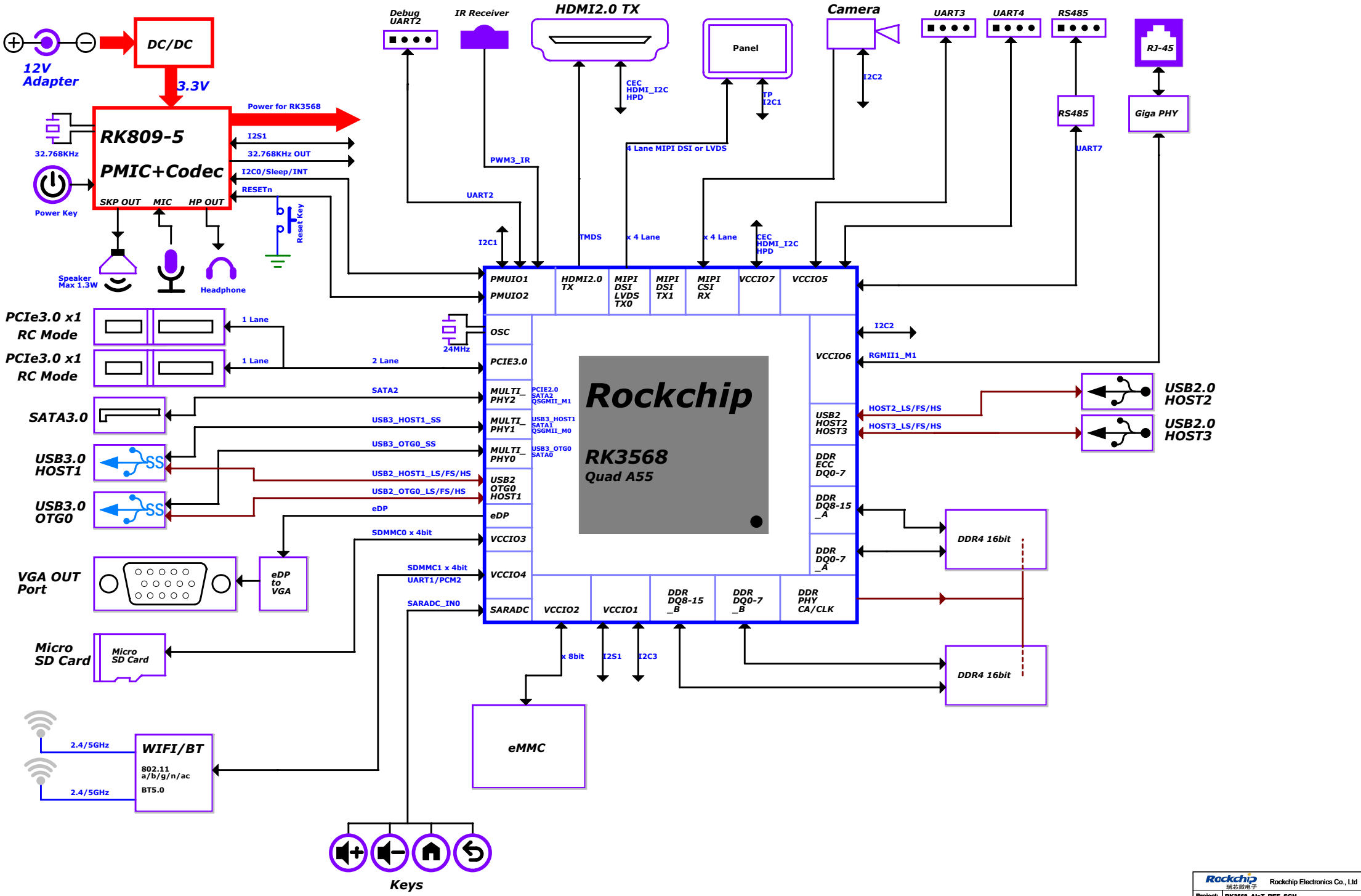
RK3568 Ref Block Diagram(Default configuration)



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Date:	Wednesday, June 16, 2021
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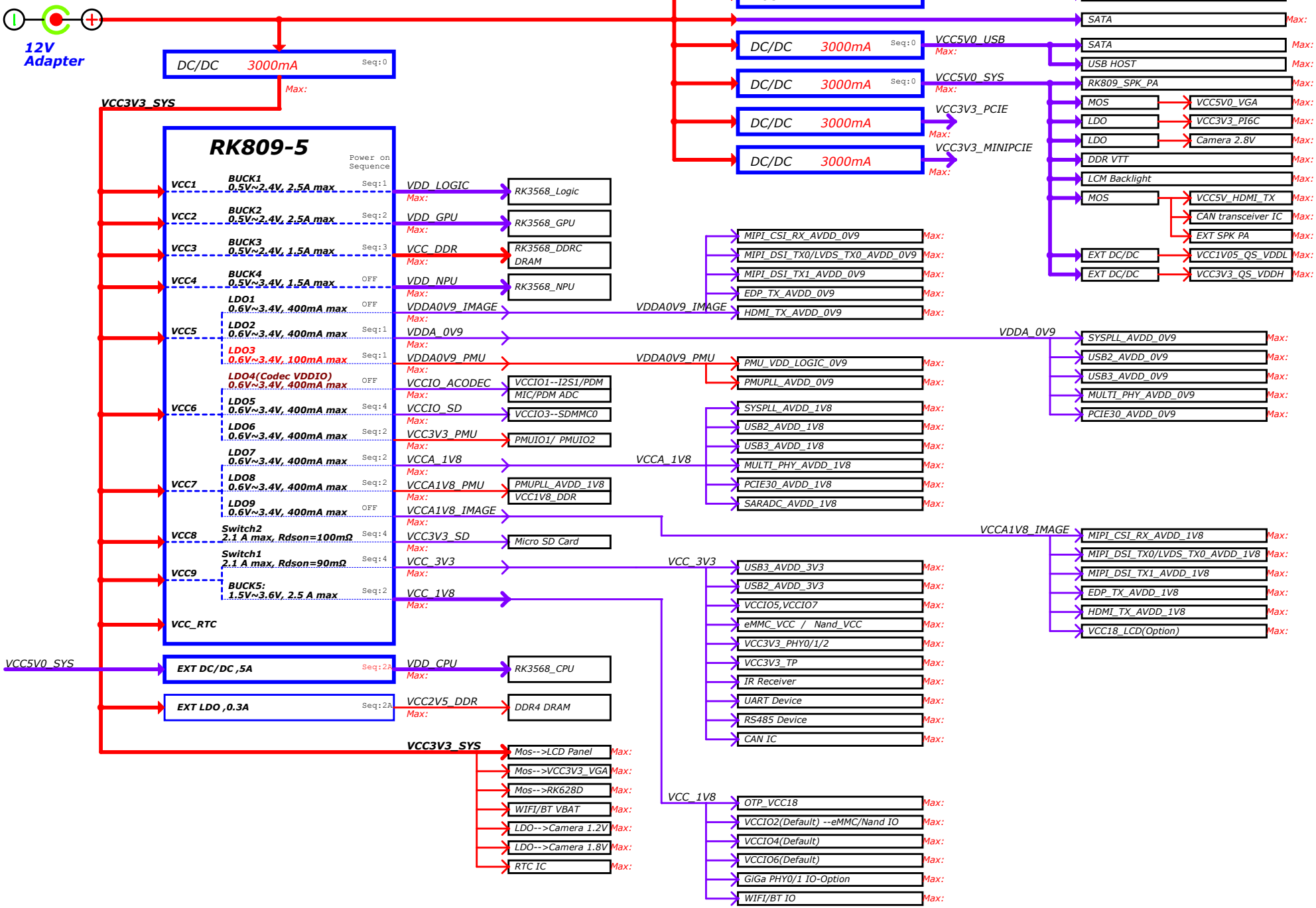
Default Power Diagram



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Date:	Wednesday, June 16, 2021
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Designed by:	Zhangtz
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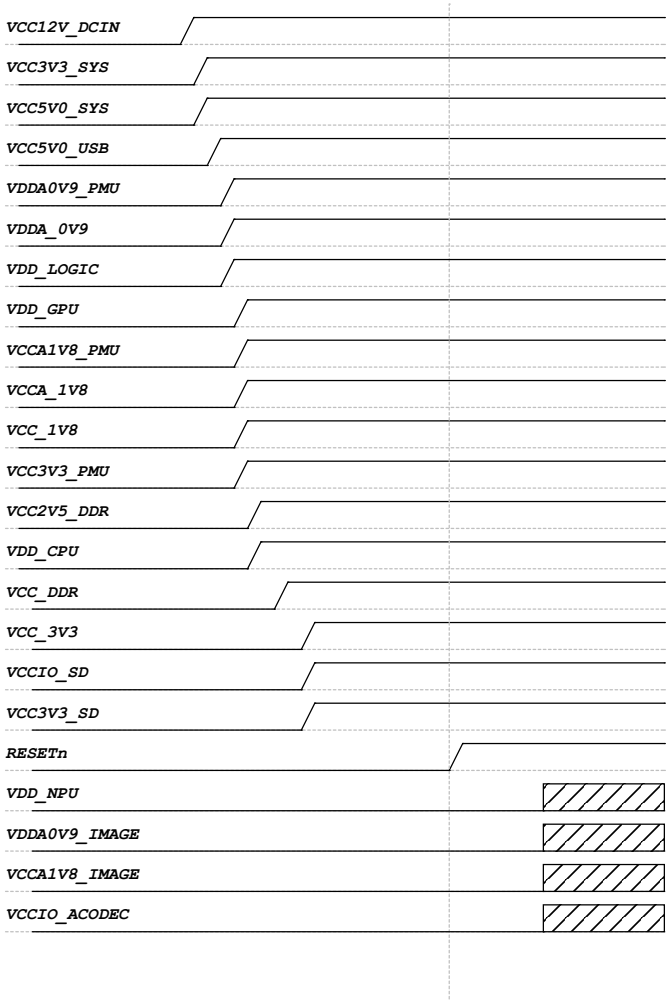
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC3V3_SYS	RK809_BUCK1	2.5A	VDD_LOGIC	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_BUCK2	2.5A	VDD_GPU	Slot:2	0.9V	ON	DVFS	TBD	TBD
VCC3V3_SYS	RK809_BUCK3	1.5A	VCC_DDR	Slot:3	ADJ FB=0.8V	ON	1.2V (DDR4)	TBD	TBD
VCC3V3_SYS	RK809_BUCK4	1.5A	VDD_NPU	N/A	0V	OFF	DVFS	TBD	TBD
VCC3V3_SYS	RK809_LDO1	0.4A	VDDA0V9_IMAGE	N/A	0V	OFF	0.9V	TBD	TBD
	RK809_LDO2	0.4A	VDDA_0V9	Slot:1	0.9V	ON	0.9V	TBD	TBD
	RK809_LDO3	0.1A	VDDA0V9_PMU	Slot:1	0.9V	ON	0.9V	TBD	TBD
VCC3V3_SYS	RK809_LDO4	0.4A	VCCIO_ACODEC	N/A	0V	OFF	3.3V	TBD	TBD
	RK809_LDO5	0.4A	VCCIO_SD	Slot:4	3.3V	ON	3.3V or 1.8V (SD2.0=3.3V,SD3.0=1.8V)	TBD	TBD
	RK809_LDO6	0.4A	VCC3V3_PMU	Slot:2	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_LDO7	0.4A	VCCA_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO8	0.4A	VCCA1V8_PMU	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_LDO9	0.4A	VCCA1V8_IMAGE	N/A	0V	OFF	1.8V	TBD	TBD
VCC3V3_SYS	RK809_SW2 100mohm	2.1A	VCC3V3_SD	Slot:4	3.3V	ON	3.3V	TBD	TBD
VCC3V3_SYS	RK809_SW1 90mohm	2.1A	VCC_3V3	Slot:4	3.3V	ON	3.3V	TBD	TBD
	RK809_BUCK5	2.5A	VCC_1V8	Slot:2	1.8V	ON	1.8V	TBD	TBD
	RK809_RESETn			Slot:4+5					
VCC12V_DCIN	EXT BUCK	3.0A	VCC3V3_SYS	Slot:0	3.3V	ON	3.3V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3.0A	VCC5V0_SYS	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC5V0_SYS	EXT BUCK	6.0A	VDD_CPU	Slot:2A	1.025V	ON	DVFS	TBD	TBD
VCC3V3_SYS	EXT LDO	0.3A	VCC2V5_DDR	Slot:2A	2.5V	ON	2.5V	TBD	TBD

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IO Power Domain Map

If IO domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

IO Domain	Pin Num	Support IO Voltage		Notes	Default IO Domain Voltage		
		3.3V	1.8V		Supply Power Net Name	Power Source	Voltage
PMUIO0 (PMUPLL_AVDD_1V8)	Pin Y21	✗	✓	PMUIO0 are fixed 1.8V level mode, which cannot be configured.	VCCA1V8_PMU	VCCA1V8_PMU	1.8V
PMUIO1	Pin Y20	✓	✗	PMUIO1 are fixed 3.3V level mode, which cannot be configured.	VCC3V3_PMU	VCC3V3_PMU	3.3V
PMUIO2	Pin W19	✓	✓	PMUIO2 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC3V3_PMU	VCC3V3_PMU	3.3V
VCCIO1	Pin H17	✓	✓	VCCIO1 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO_ACODEC	VCCIO_ACODEC	3.3V
VCCIO2	Pin H18	✓	✓	VCCIO2 supports 1.8V or 3.3V level mode Default is configured by hardware,namely PIN "FLASH_VOL_SEL" state determines which mode to work in.[1][2]	VCCIO_FLASH	VCC_1V8	1.8V
VCCIO3	Pin L22	✓	✓	VCCIO3 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2][3]	VCCIO_SD	VCCIO_SD	3.3V
VCCIO4	Pin J21	✓	✓	VCCIO4 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO4	VCC_1V8	1.8V
VCCIO5	Pin V10 Pin V11	✓	✓	VCCIO5 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V
VCCIO6	Pin R9 Pin U9	✓	✓	VCCIO6 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCCIO6	VCC_1V8	1.8V
VCCIO7	Pin V12	✓	✓	VCCIO7 supports 1.8V or 3.3V level mode Support configurable but require that their hardware power supply voltages must be consistent with the software configuration correspondingly.[2]	VCC_3V3	VCC_3V3	3.3V

For example, the VCCIO4 hardware has been modified to 3.3V power supply, and the corresponding DTS must be modified to 3.3V configuration, otherwise the IO of VCCIO4 will be damaged.

If a board needs to be compatible with two voltage choices, recommended to enable BOM ID

Notes

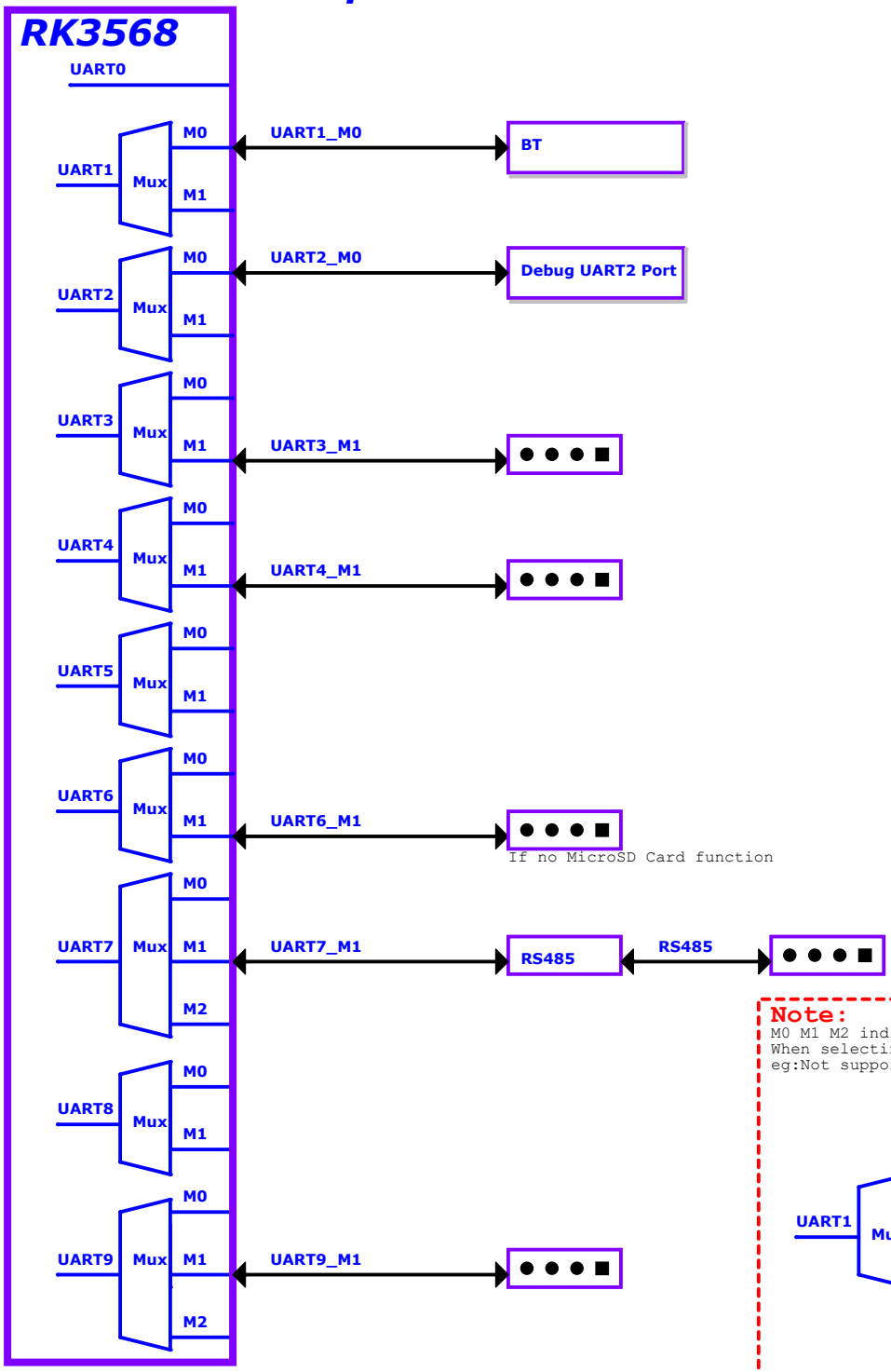
[1]:When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

[2]:When the IO domain power supply voltage is 1.8V, the IO domain voltage configuration in DTS must be set to 1.8V mode.
If it is misconfigured to 3.3V mode, the IO function of this power domain will be abnormally;
When the IO domain power supply voltage is 3.3V, the IO domain voltage configuration in DTS must be set to 3.3V mode.
If it is misconfigured to 1.8V mode, the IO in this power domain will be in overvoltage state, and the IO will be damaged after long-term operation.

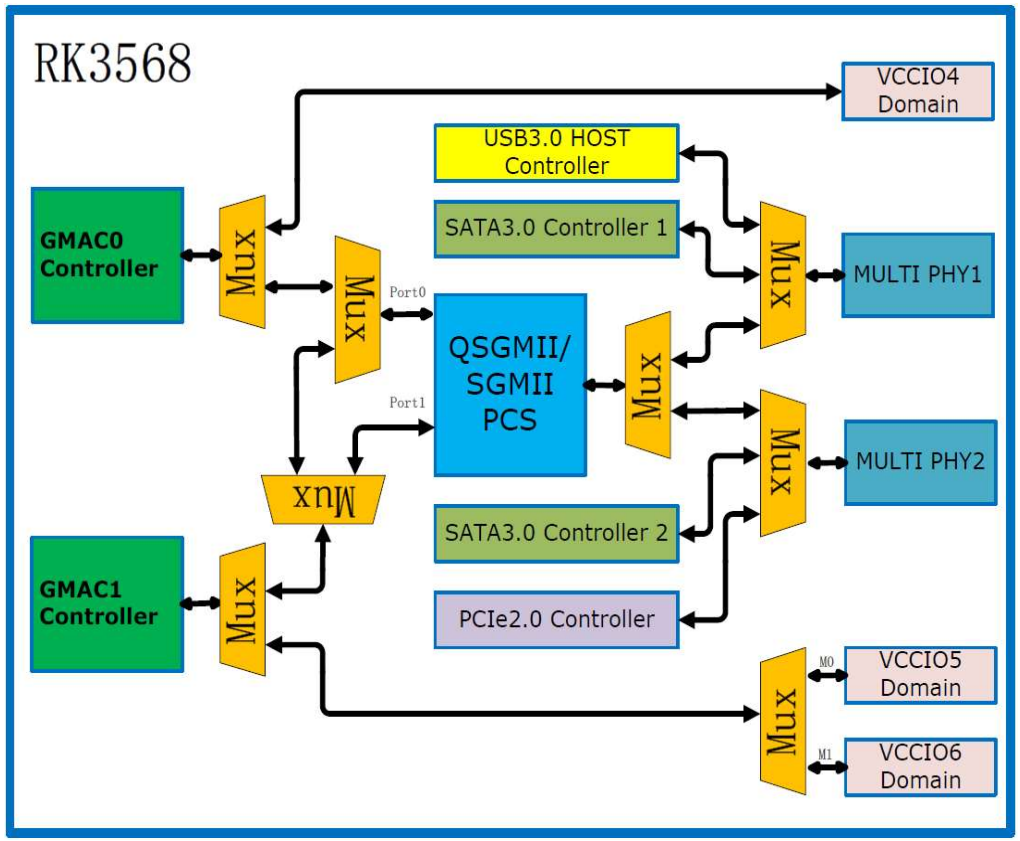
[3]:When VCCIO3 IO domain is assigned as SD card function,:
If SD3.0 mode is to be supported, VCCIO3 power supply voltage must be support configurable, 3.3V in SD2.0 mode and 1.8V in SD3.0 mode.
If only SD2.0 mode is supported (SD3.0 card only works in SD2.0 mode), VCCIO3 only needs fixed power supply of 3.3V.
When VCCIO3 IO domain is assigned as other function,:
Such as uart5 and uart6, then note [2] should be followed

Default UART Map

RK3568

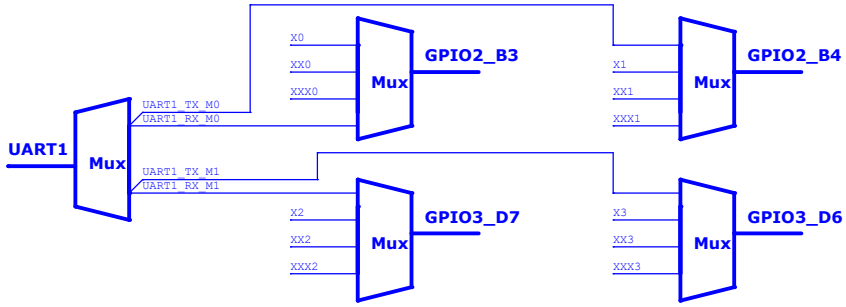


GMAC0/1 Path Map



Note:

M0 M1 M2 indicates that the same function is multiplexed to different IO
When selecting, only M0 or M1 or M2 can be selected
eg:Not supported UART1_TX_M0 and UART1_RX_M1 combination



It is suitable for other interfaces

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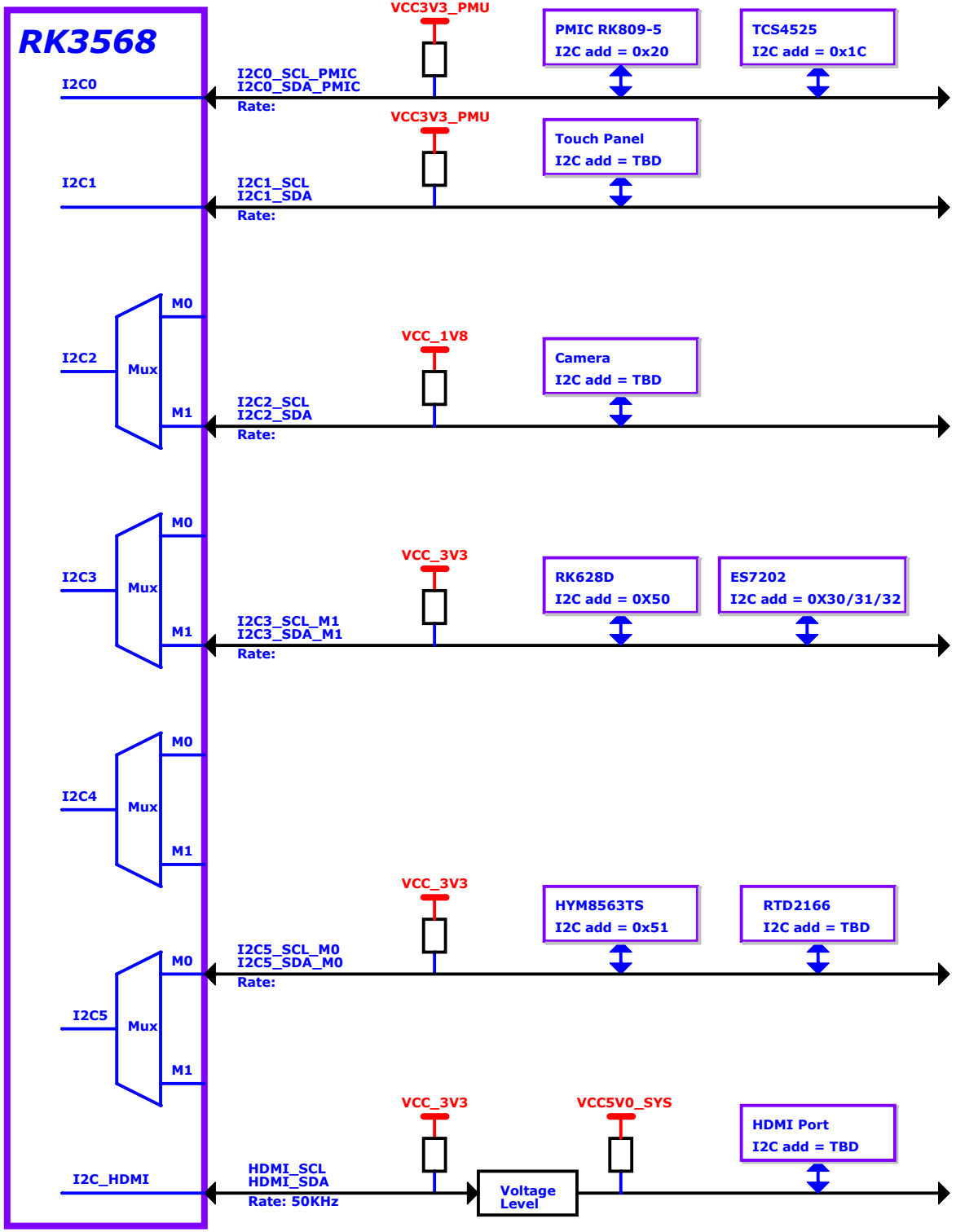
Default I2C Map

Note:
M0 M1 M2 indicates that the same function is multiplexed to different IO. When selecting, only M0 or M1 or M2 can be selected
eg:
Not supported I2C1_SCL_M0 and I2C1_SDA_M1 combination



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File:	08.I2C Bus Map				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
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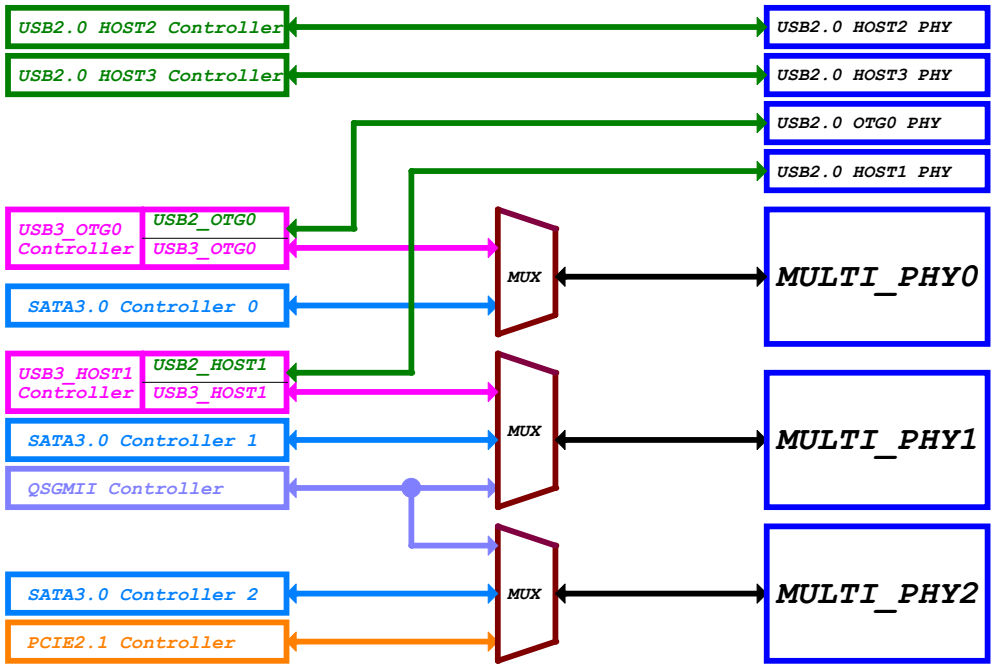
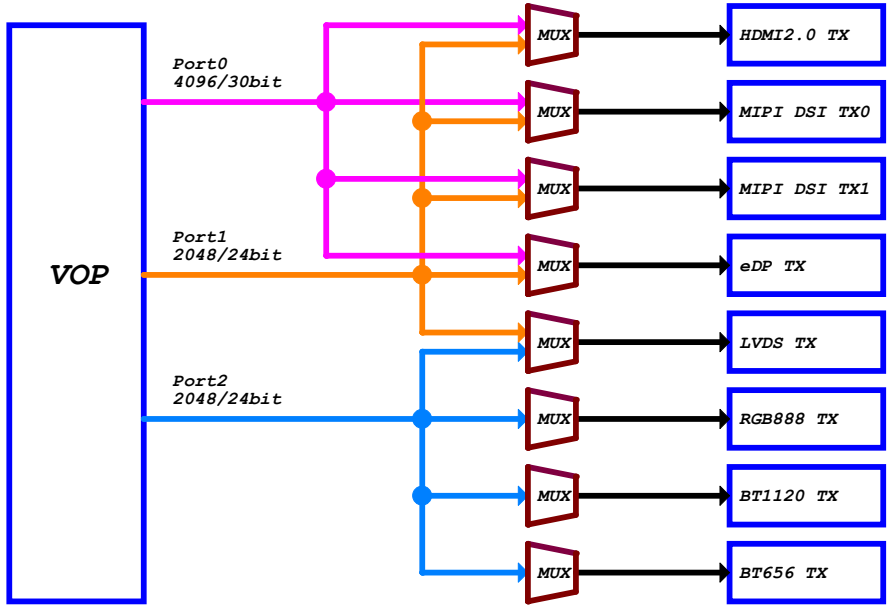
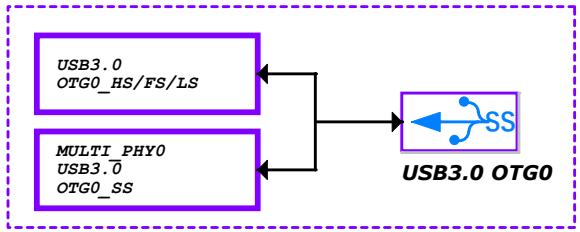
MULTI_PHY0/1/2 Path Map



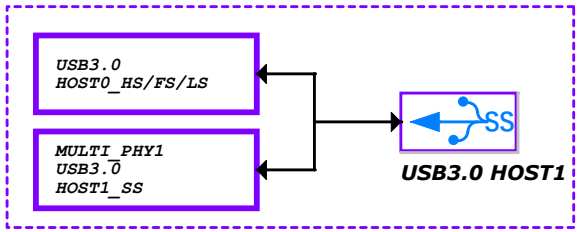
VOP Path Map



USB3.0 OTG0



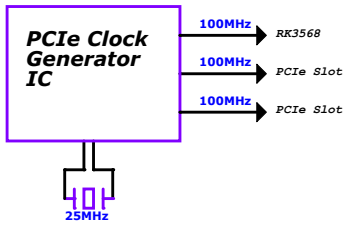
USB3.0 HOST1



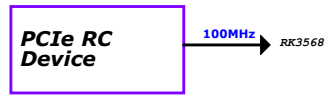
PCIe3.0 PHY

Option1	PCIe3.0 x2Lane	PCIE30_REFCLK (RC/EP:input)	PCIE30_TX0 PCIE30_RX0 PCIE30_TX1 PCIE30_RX1	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	RC or EP
Option2	PCIe3.0 x1Lane + PCIe3.0 x1Lane	PCIE30_REFCLK (RC:input)	PCIE30_TX0 PCIE30_RX0	PCIE30X2_CLKREQn PCIE30X2_WAKEn PCIE30X2_PERSTn PCIE30X2_BUTTONRSTn	Only RC
			PCIE30_TX1 PCIE30_RX1	PCIE30X1_CLKREQn PCIE30X1_WAKEn PCIE30X1_PERSTn PCIE30X1_BUTTONRSTn	Only RC

PCIe3.0 REFCLK-RC Mode



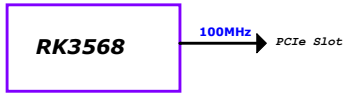
PCIe3.0 REFCLK-EP Mode



PCIe2.1 PHY

MULTI_PHY2	PCIe2.1 x1Lane	PCIE20_REFCLK (RC:output)	PCIE20_TX PCIE20_RX	PCIE20_CLKREQn PCIE20_WAKEn PCIE20_PERSTn PCIE20_BUTTONRSTn	Only RC

PCIe2.1 REFCLK-RC Mode



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File:	09.PCIE30/MULTI_PHY/VOP Fun Map
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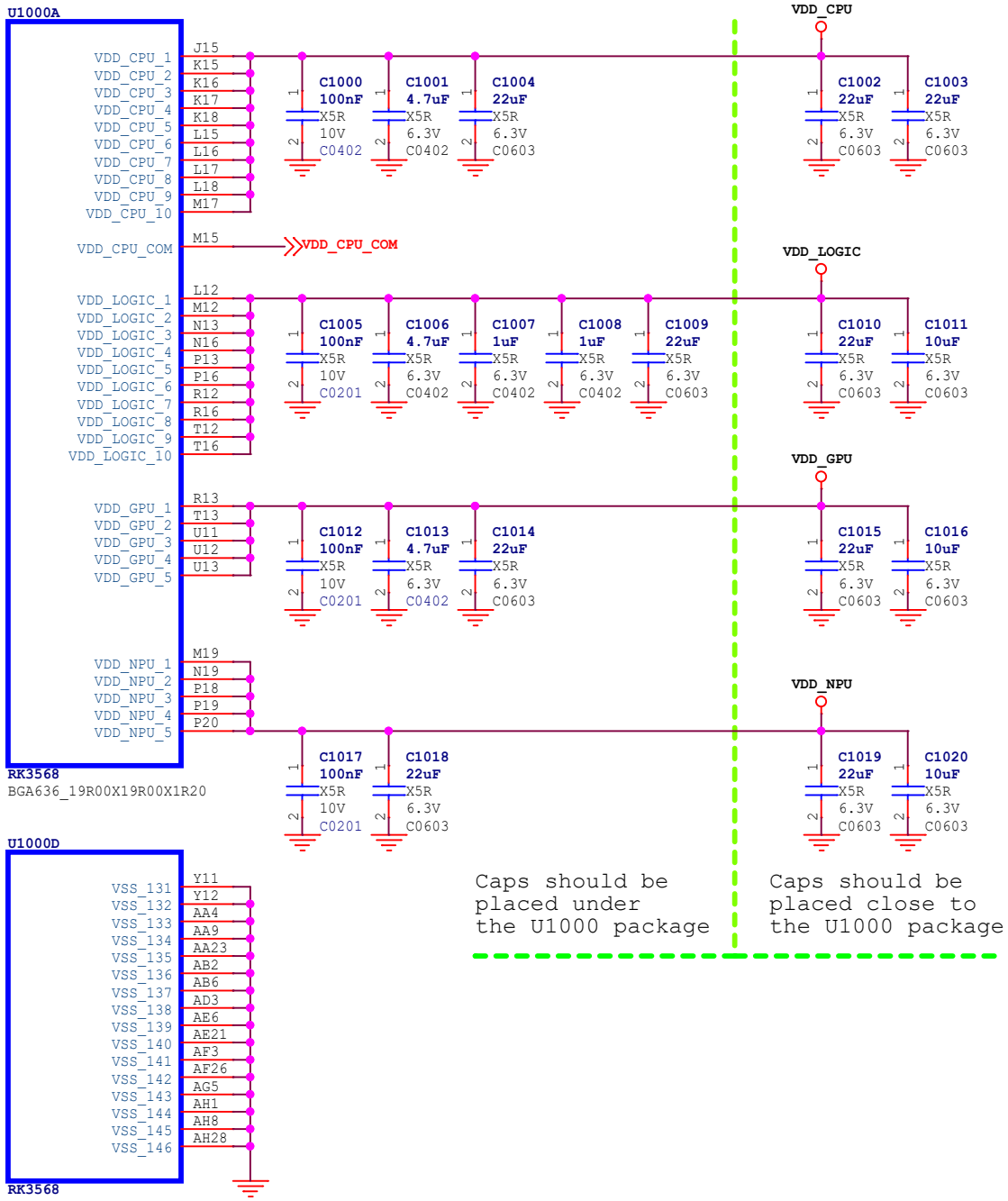
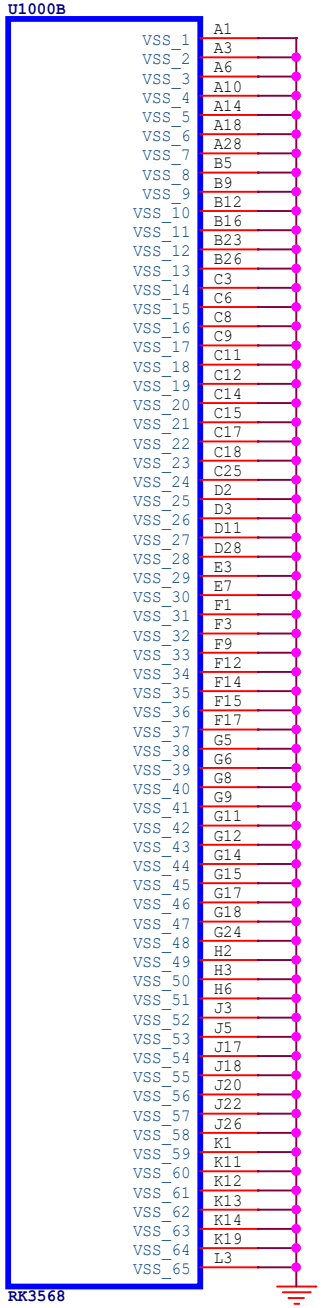
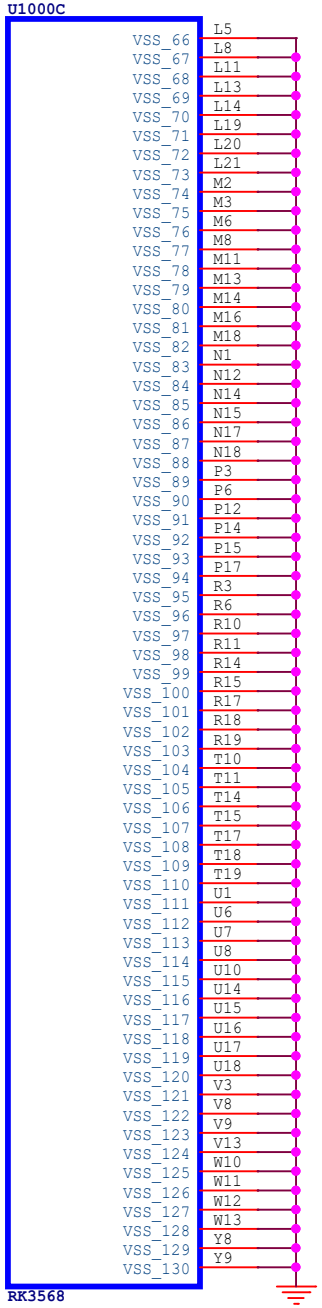
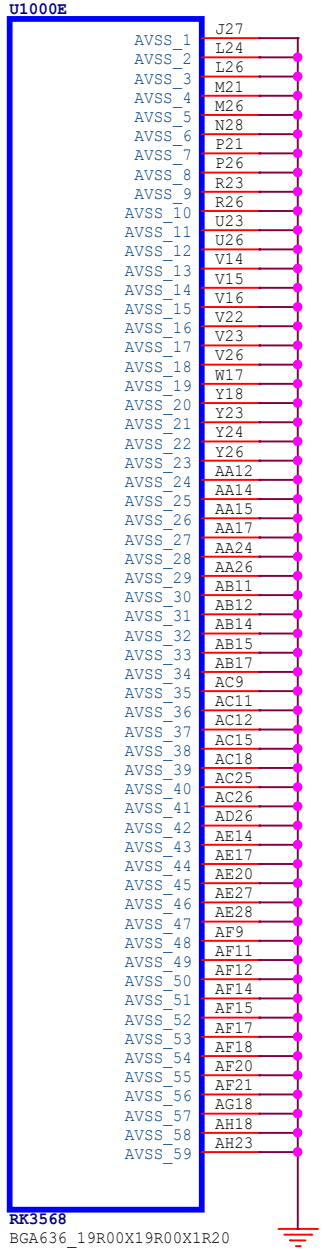
RK3568_ABCDE (Power&Gnd)









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Project:	RK3568_AIoT_REF_SCH				
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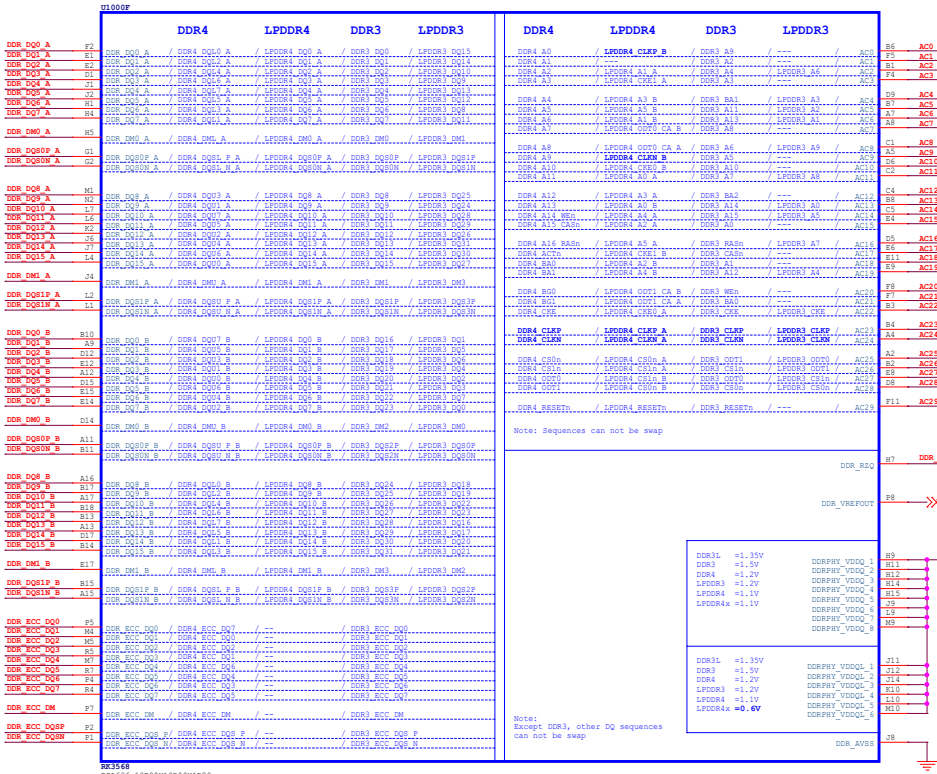
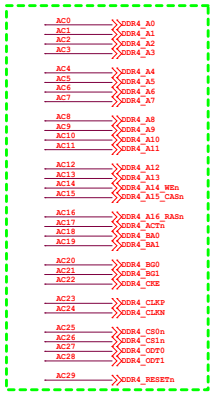
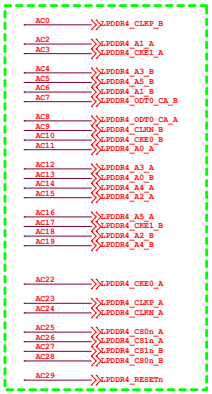
RK3568_F (DDR PHY)



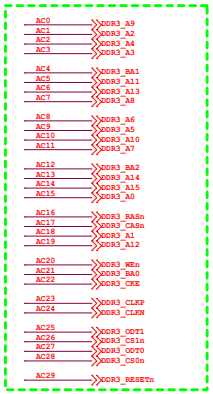
Default DDR4 AC



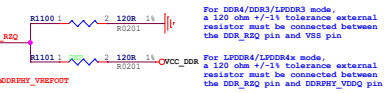
LPDDR4/4x AC

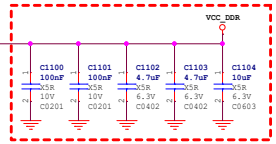


DDR3 AC



LPDDR3 AC

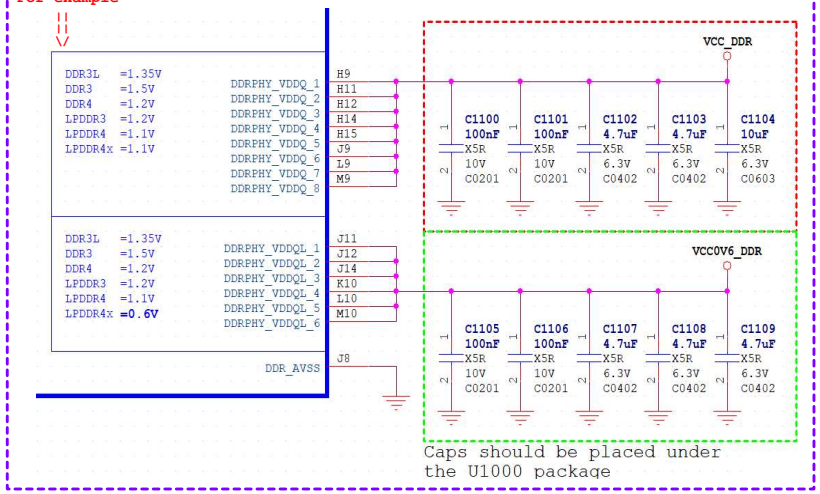




Default DDR4

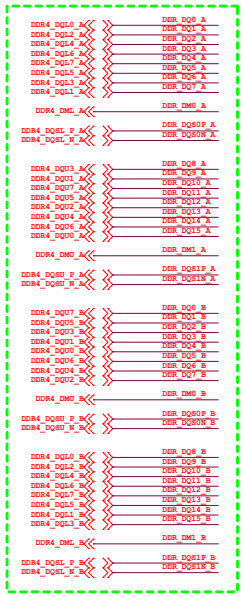
Note:
Caps should be placed under the U1000 package

Note:
LPDDR4x mode:
Pin J11,J12,J14,K10,L10,M10 connected to VCC0V6_DDR power supply
For example



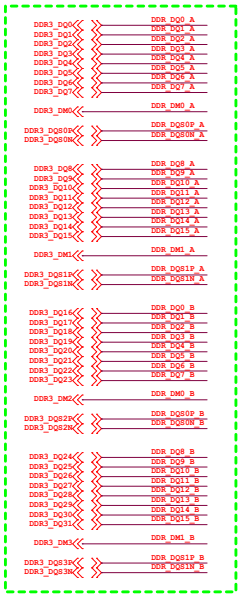
Caps should be placed under the U1000 package

Default DDR4 DQ

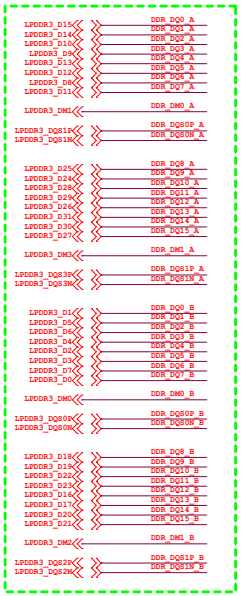


LPDDR4/4x DQ

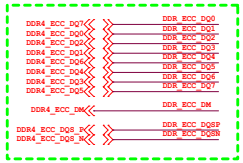
DDR3 DQ



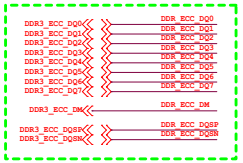
LPDDR3 DQ



DDR4 ECC DQ



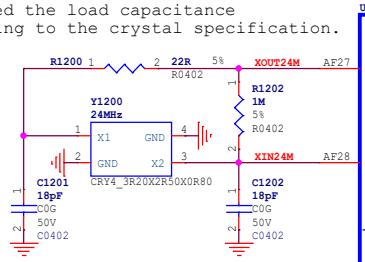
DDR3 ECC DQ

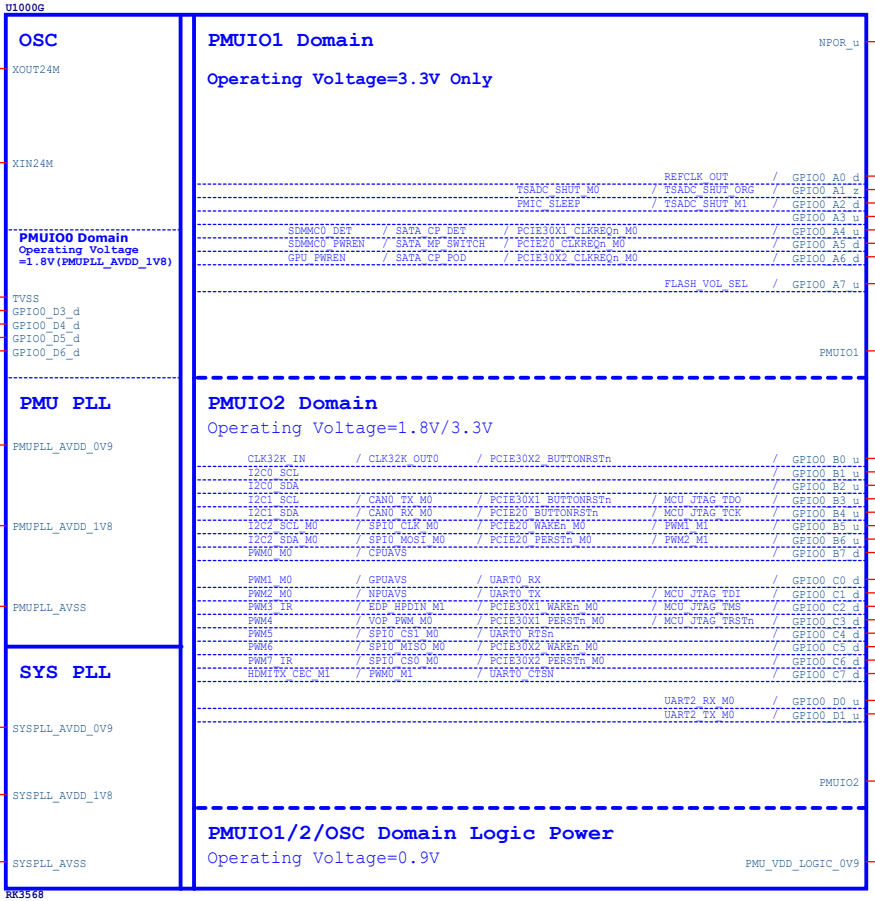


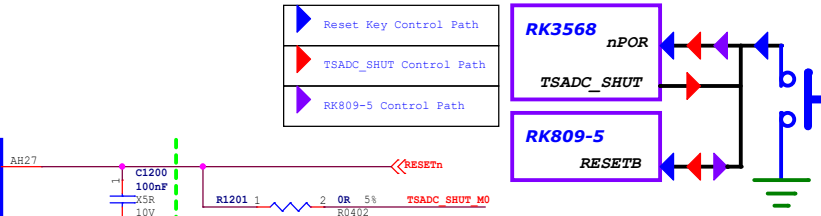
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	11.RK3568_DDR PHY		
Date:	Wednesday, June 16, 2021	Rev:	V1.1
Designed by: Zhangtz	Reviewed by: Default	Sheet:	12 of 72

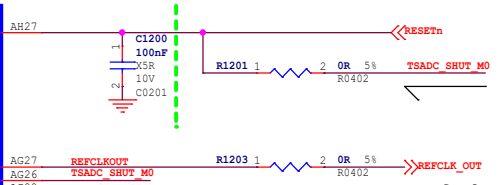
RK3568_G(OSC/PLL/PMUIO1/2)

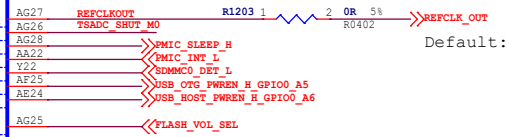
Note:
Adjusted the load capacitance according to the crystal specification.

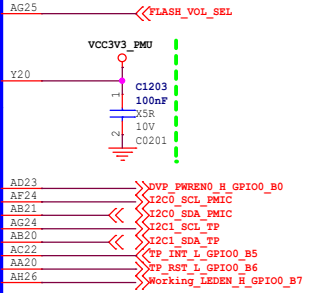


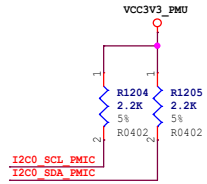


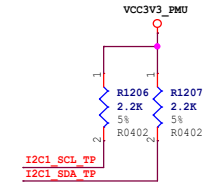


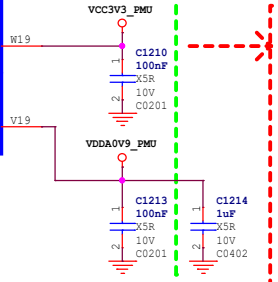


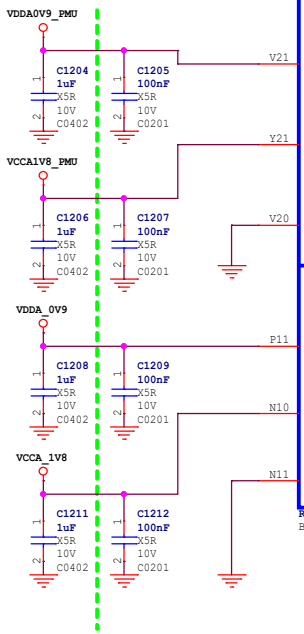












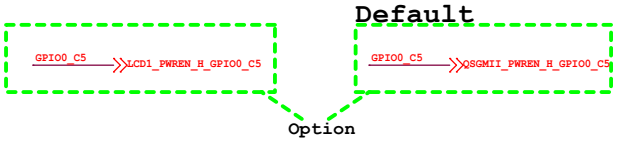
Note:
If PMUIO2 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the PMUIO2 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of PMUIO2 will be abnormally.

The PMUIO2 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of PMUIO2 will be damaged!

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package



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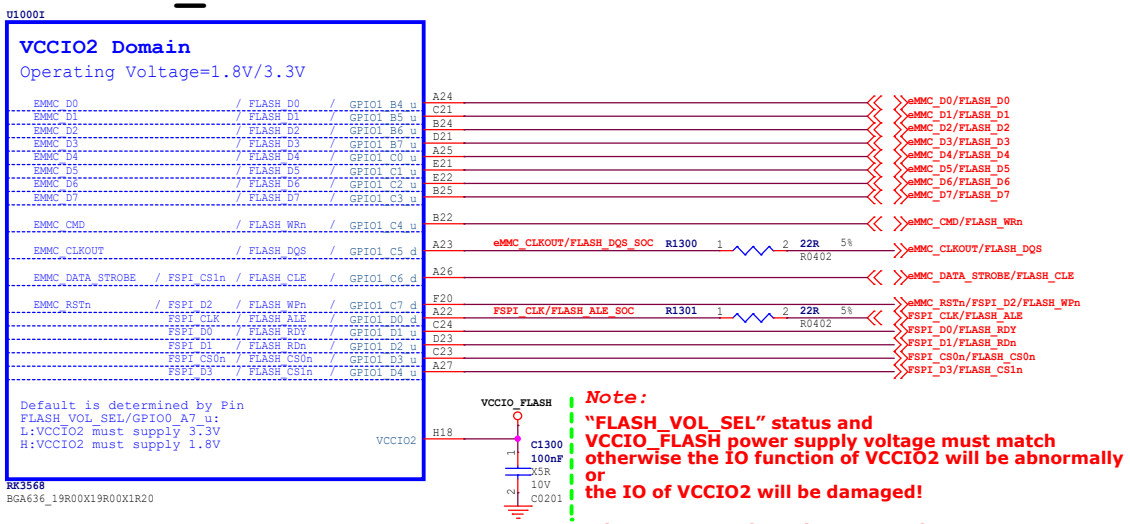
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	12.RK3568_OSC/PLL/PMUIO				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	13 of 72

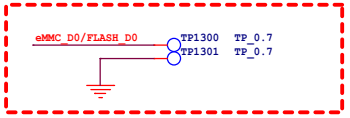
RK3568_I(VCCIO2 Domain)



Note:

"FLASH_VOL_SEL" status and VCCIO_FLASH power supply voltage must match otherwise the IO function of VCCIO2 will be abnormally or the IO of VCCIO2 will be damaged!

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship, its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

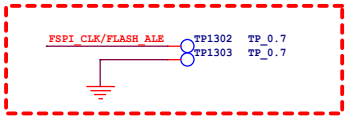


Note:

For eMMC or Nand Flash:
If eMMC_D0/FLASH_D0=0V at after power on and reset, then system will enter into Maskrom mode.

Layout note:

Test point must be placed on the line, and no branch can be added



Note:

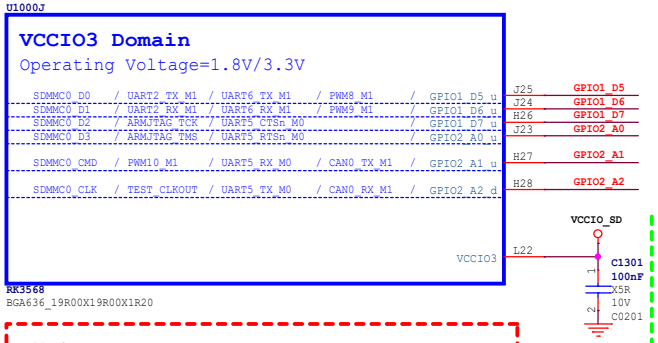
For SPI Flash:
If FSPI_CLK=0V at after power on and reset, then system will enter into Maskrom mode.

Note:

Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure, use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)

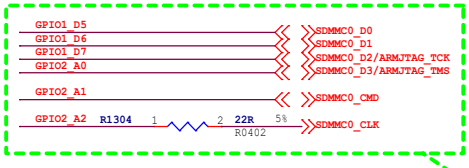


Note:

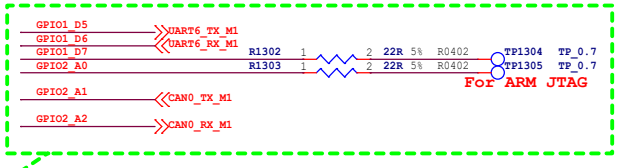
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Default

SDMMC0&JTAG



UART&CAN&JTAG



Option

Note:

If VCCIO3 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

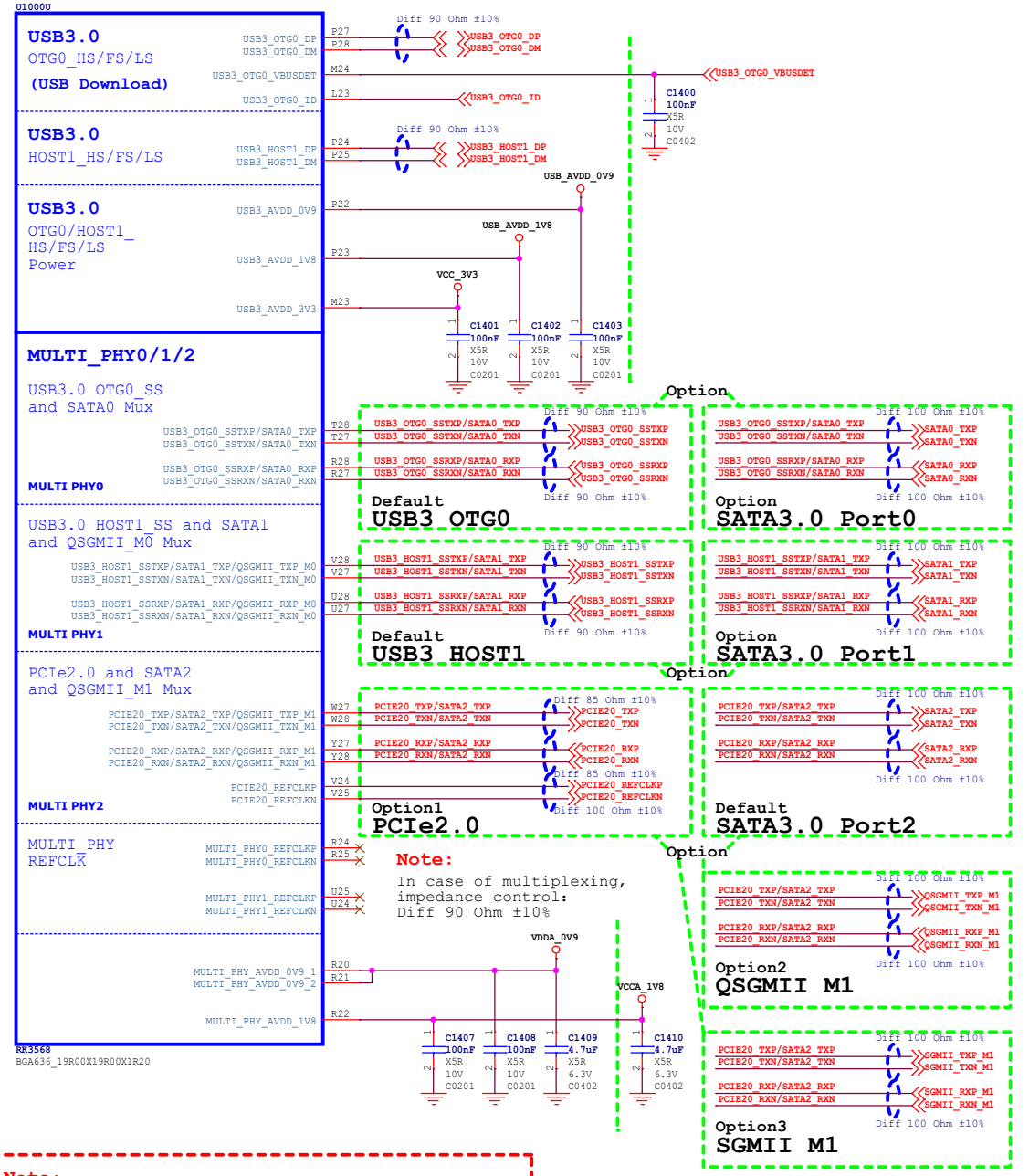
If the VCCIO3 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO3 will be abnormally.

The VCCIO3 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO3 will be damaged!

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	13.RK3568_Flash/SD Controller				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	14 of 72

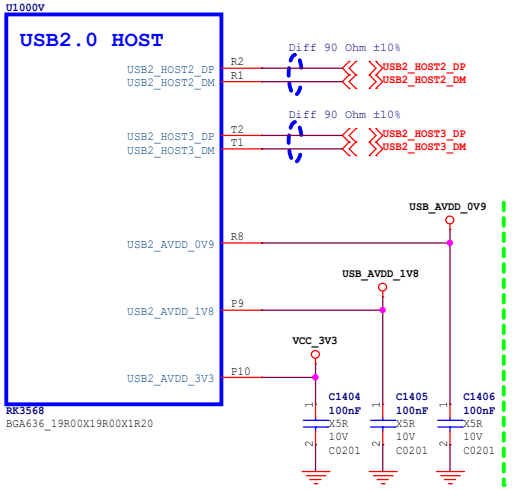
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



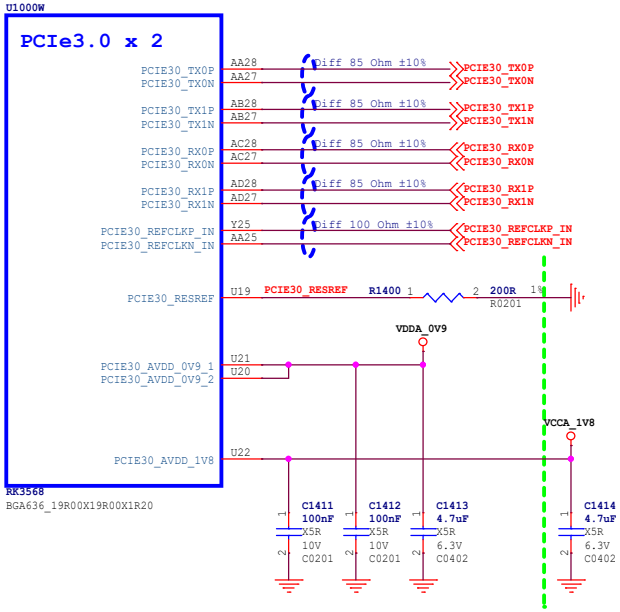
Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Rockchip Confidential

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	14.RK3568_USB/PCIe/SATA PHY				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	15 of 72

RK3568_K(VCCIO4 Domain)

Note: *If VCCIO4 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!*
If the VCCIO4 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO4 will be abnormally.
The VCCIO4 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO4 will be damaged!

U1000K

VCCIO4 Domain
Operating Voltage=1.8V/3.3V

SDMMC1_D0	GMAC0_RXD2	UART6_RX_M0		GPIO2_A3_u
SDMMC1_D1	GMAC0_RXD3	UART6_TX_M0		GPIO2_A4_u
SDMMC1_D2	GMAC0_RXCLK	UART7_RX_M0		GPIO2_A5_u
SDMMC1_D3	GMAC0_TXD2	UART7_TX_M0		GPIO2_A6_u
SDMMC1_CMD	GMAC0_TXD3	UART9_RX_M0		GPIO2_A7_u
SDMMC1_CLK	GMAC0_TXCLK	UART9_TX_M0		GPIO2_B0_d
SDMMC1_PWREN	I2C4_SDA_M1	UART8_RTSn_M0	CAN2_RX_M1	GPIO2_B1_d
SDMMC1_DET	I2C4_SCL_M1	UART8_CTSn_M0	CAN2_TX_M1	GPIO2_B2_u
	GMAC0_TXD0	UART1_RX_M0		GPIO2_B3_u
	GMAC0_TXD1	UART1_TX_M0		GPIO2_B4_u
	GMAC0_TXEN	UART1_RTSn_M0	SPI1_CLK_M0	GPIO2_B5_u
	GMAC0_RXD0	UART1_CTSn_M0	SPI1_MISO_M0	GPIO2_B6_u
I2S2_SCLK_RX_M0	GMAC0_RXD1	UART6_RTSn_M0	SPI1_MOSI_M0	GPIO2_B7_d
I2S2_LRCK_RX_M0	GMAC0_RXDV_CRS	UART6_CTSn_M0	SPI1_CS0_M0	GPIO2_C0_d
I2S2_MCLK_M0	ETH0_REFCLKO_25M	UART7_RTSn_M0	SPI1_CLK_M0	GPIO2_C1_d
I2S2_SCLK_TX_M0	GMAC0_MCLKINOUT	UART7_CTSn_M0	SPI2_MISO_M0	GPIO2_C2_d
I2S2_LRCK_TX_M0	GMAC0_MDC	UART9_RTSn_M0	SPI2_MOSI_M0	GPIO2_C3_d
I2S2_SDO_M0	GMAC0_MDIO	UART9_CTSn_M0	SPI2_CS0_M0	GPIO2_C4_d
I2S2_SDI_M0	GMAC0_RXER	UART8_TX_M0	SPI2_CS1_M0	GPIO2_C5_d
CLK32K_OUT1		UART8_RX_M0	SPI1_CS1_M0	GPIO2_C6_d

VCCIO4 — J21 — C1500 100nF X5R 10V C0201

RK3568
BGA636_19R00X19R00X1R20

Default

WIFI+BT+PCM

GPIO2_A3 SDMMC1_D0
GPIO2_A4 SDMMC1_D1
GPIO2_A5 SDMMC1_D2
GPIO2_A6 SDMMC1_D3
GPIO2_A7 SDMMC1_CMD
GPIO2_B0 — R1502 22R 5% R0402 — SDMMC1_CLK
GPIO2_B1 WIFI_REG_ON_H_GPIO2_B1
GPIO2_B2 WIFI_WAKE_HOST_H_GPIO2_B2
GPIO2_B3 UART1_RX_M0
GPIO2_B4 UART1_TX_M0
GPIO2_B5 UART1_RTSn_M0
GPIO2_B6 UART1_CTSn_M0
GPIO2_B7 BT_REG_ON_H_GPIO2_B7
GPIO2_C0 BT_WAKE_HOST_H_GPIO2_C0
GPIO2_C1 HOST_WAKE_BT_H_GPIO2_C1
GPIO2_C2 SOC_PCM_CLK
GPIO2_C3 SOC_PCM_SYNC
GPIO2_C4 SOC_PCM_OUT
GPIO2_C5 SOC_PCM_IN
GPIO2_C6 — R1508 0R 5% R0402 — CLK32K_OUT1_WIFI

VCCIO4 — R1510 0R 5% R0402 — VCCIO_WL

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Option

RGMII0

GPIO2_A3 GMAC0_RXD2
GPIO2_A4 GMAC0_RXD3
GPIO2_A5 GMAC0_RXCLK
GPIO2_A6 — R1500 22R 5% R0402 — GMAC0_TXD2
GPIO2_A7 — R1501 22R 5% R0402 — GMAC0_TXD3
GPIO2_B0 — R1503 22R 5% R0402 — GMAC0_TXCLK
GPIO2_B3 — R1504 22R 5% R0402 — GMAC0_TXD0
GPIO2_B4 — R1505 22R 5% R0402 — GMAC0_TXD1
GPIO2_B5 — R1506 22R 5% R0402 — GMAC0_TXEN
GPIO2_B6 GMAC0_RXD0
GPIO2_B7 GMAC0_RXD1
GPIO2_C0 GMAC0_RXDV_CRS
GPIO2_C1 — R1507 22R 5% R0402 — ETH0_REFCLKO_25M
GPIO2_C2 GMAC0_MCLKINOUT
GPIO2_C3 — R1513 0R 5% R0402 — GMAC0_MDC
GPIO2_C4 GMAC0_MDIO
GPIO2_C5 GMAC0_RXER

V1.1

VCCIO4
R1509 0R 5% R0402 — VCC_1V8
R1511 DNP 0R 5% R0402 — VCC_3V3

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

GMAC0_TXEN — R1515 4.7K 5% R0402 DNP

Note:
According to the actual choice of mounted Cannot be mounted at the same time
Default:1.8V
Select the voltage according to the application

RTL8201F/YT8512C only support 3.3V IO
VCCIO4 must be changed to 3.3V power supply

RK3568_N(VCCIO7 Domain)

Note:
When use HDMI, HDMITX_SCL/SDA cannot be shared with other devices

U1000N

VCCIO7 Domain
Operating Voltage=1.8V/3.3V

PWM14_M1	SPI3_CLK_M1	CAN1_RX_M1	PCIE30X2_CLKREQn_M2	I2S3_MCLK_M1	GPIO4_C2_d
PWM15_IR_M1	SPI3_MOSI_M1	CAN1_TX_M1	PCIE30X2_WAKEn_M2	I2S3_SCLK_M1	GPIO4_C3_d
EDP_HPDIN_M0	SPDIF_TX_M2	SATA2_ACT_LED	PCIE30X2_PERSTn_M2	I2S3_LRCK_M1	GPIO4_C4_d
PWM12_M1	SPI3_MISO_M1	SATA1_ACT_LED	UART9_TX_M1	I2S3_SDO_M1	GPIO4_C5_d
PWM13_M1	SPI3_CS0_M1	SATA0_ACT_LED	UART9_RX_M1	I2S3_SDI_M1	GPIO4_C6_d
HDMITX_SCL	I2C5_SCL_M1				GPIO4_C7_u
HDMITX_SDA	I2C5_SDA_M1				GPIO4_D0_u
HDMITX_CEC_M0	SPI3_CS1_M1				GPIO4_D1_u
					GPIO4_D2_d

AF8 4G_DISABLE_GPIO4_C2
AA11 HDMIRX_INT_L_GPIO4_C3
AH7 SATA2_ACT_LED
AD8 GPIO4_C5
AE8 GPIO4_C6
AG8 HDMITX_SCL
AG7 HDMITX_SDA
AH6 HDMITX_CEC_M0
AB9 HDMIRX_RST_L_GPIO4_D2

VCCIO7 — V12 — VCC_3V3 — C1509 100nF X5R 10V C0201

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
If VCCIO7 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO7 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO7 will be abnormally.

The VCCIO7 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO7 will be damaged!

Default

GPIO4_C5 UART9_TX_M1
GPIO4_C6 UART9_RX_M1

GPIO4_C5 SATA1_ACT_LED
GPIO4_C6 SATA0_ACT_LED

Option

RK3568_O(SARADC/OTP)

U1000O

SARADC

Recovery/ SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY	C1501 1nF X5R 50V C0402
SARADC_VIN1	C26	SARADC_VIN1_HW_ID	C1502 1nF X5R 50V C0402
SARADC_VIN2	D24	SARADC_VIN2_HP_HOOK	C1503 1nF X5R 50V C0402
SARADC_VIN3	E23	SARADC_VIN3_BOM_ID	C1504 1nF X5R 50V C0402
SARADC_VIN4	G21	SARADC_VIN4	C1505 1nF X5R 50V C0402
SARADC_VIN5	F22	SARADC_VIN5	C1506 1nF X5R 50V C0402
SARADC_VIN6	G20	SARADC_VIN6	C1507 1nF X5R 50V C0402
SARADC_VIN7	F21	SARADC_VIN7	C1508 1nF X5R 50V C0402
SARADC_AVDD_1V8	H22		C1510 100nF X5R 10V C0201
OTP_VCC18	H20		C1511 100nF X5R 10V C0201

VCCA_1V8
VCC_1V8

RK3568
BGA636_19R00X19R00X1R20

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:
Must be mounted

VCCA_1V8 — R1512 10K 1% R0402 — SARADC_VIN0_KEY/RECOVERY

SARADC_VIN0_KEY/RECOVERY — TP1501 TP_0.7
TP1502 TP_0.7

Note:
If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

SARADC_VIN0_KEY/RECOVERY
SARADC_VIN1_HW_ID
SARADC_VIN2_HP_HOOK
SARADC_VIN3_BOM_ID
SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

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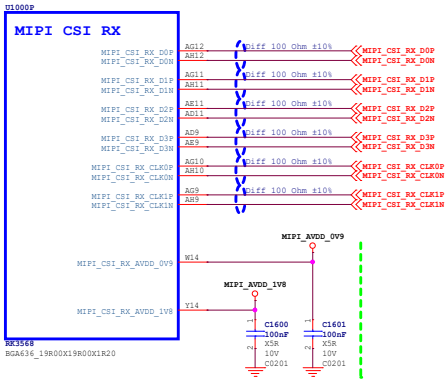
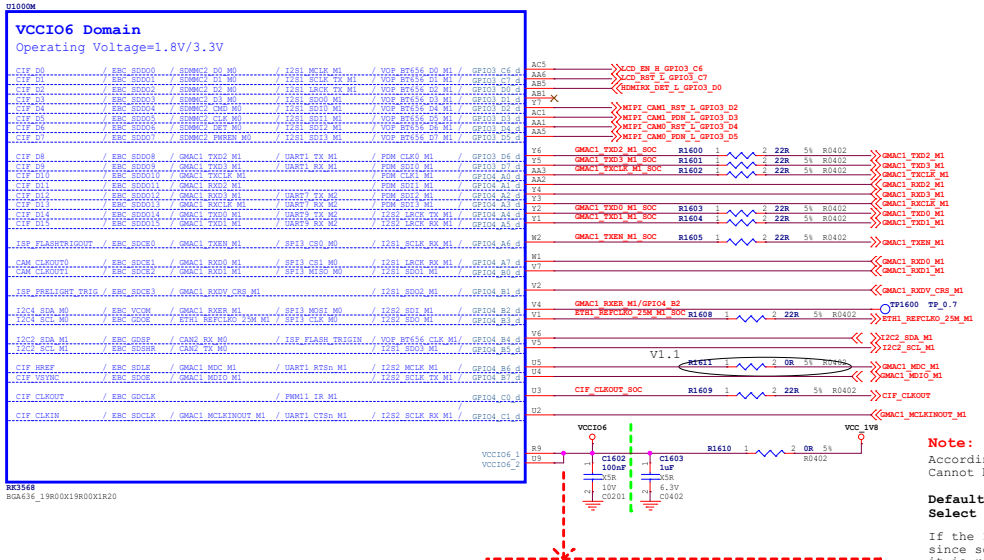
Project:	RK3568_AIoT_REF_SCH				
File:	15.RK3568_SARADC/GPIO				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	16 of 72

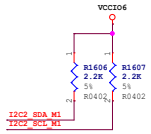
RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0
		MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)





Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
If VCCIO6 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO6 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO6 will be abnormally.

The VCCIO6 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO6 will be damaged!

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Default:1.8V
Select the voltage according to the application

If the IO domain is to be used as FEPHY,
since some FEPHY only support 3.3V IO,
it is recommended to reallocate GPIO
to reduce the cost of level conversion

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_CRS_DV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------->	PHYx_MDIO	GMACx_MDIO	<------->	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx OSC	ETHx_REFCLKO_25M	------->	PHYx OSC
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	<------->	PHYx_TXC
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

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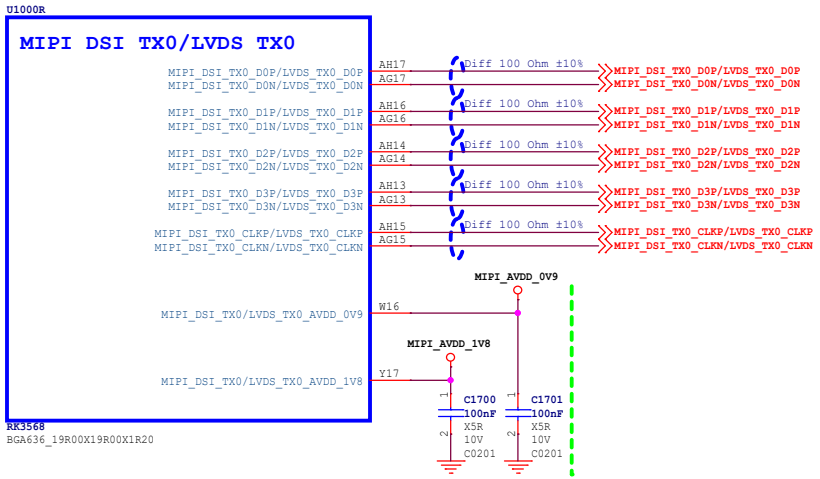
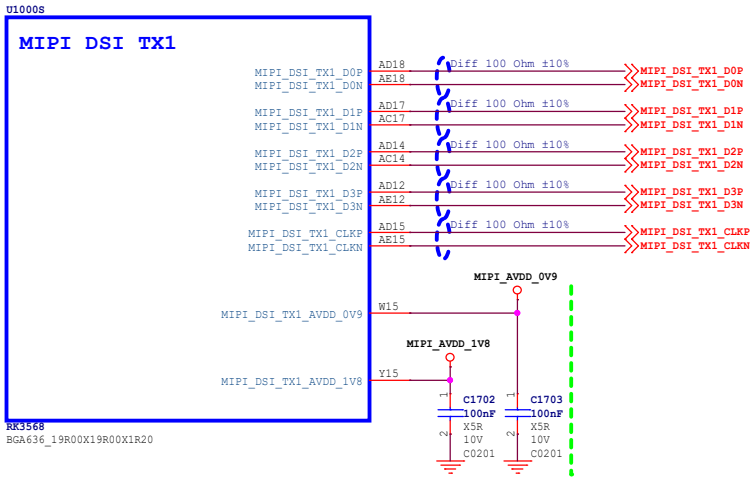
Project:	RK3568_AIoT_REF_SCH				
File:	16.RK3568_VI Interface				
Date:	Wednesday, June 16, 2021		Rev:	V1.1	
Designed by:	Zhangtz	Reviewed by:	Default	Sheet:	17 of 72

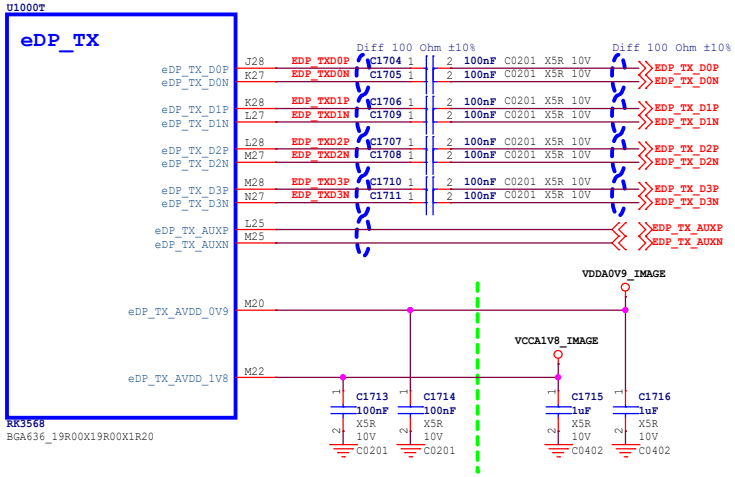
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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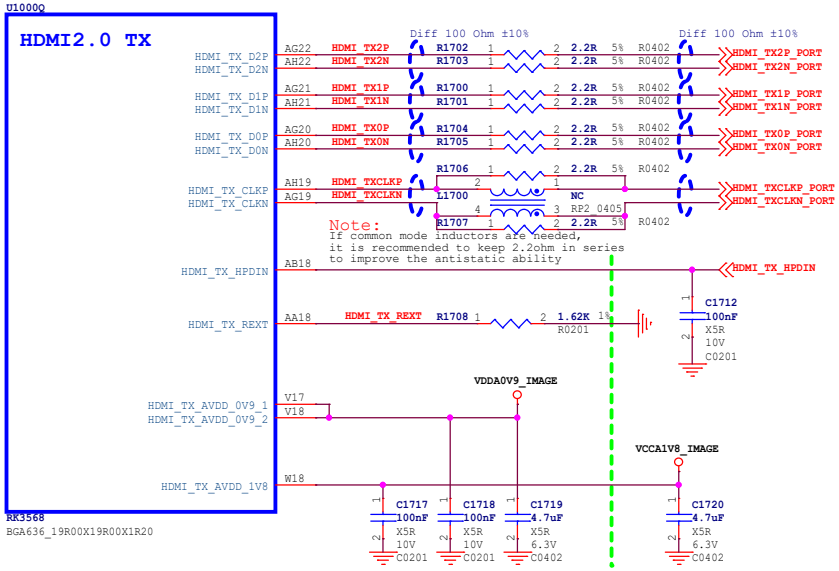
RK3568_Q(HDMI2.0 TX)



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	17.RK3568_VO Interface_1				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	18 of 72

RK3568_L(VCCIO5 Domain)

U1000L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

RK3568
BGA636_19R00X19R00X1R20

AG6 PCIE20_CLKREQn_M1
AD7 PCIE20_WAKEn_M1
AC8 PCIE30X1_CLKREQn_M1
AC7 PCIE30X1_WAKEn_M1
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 PCIE30X2_PRSNT_L_GPIO2_D7

AH4 PCIE30X1_PRSNT_L_GPIO3_A0

AB8 PCIE30X1_PERSTn_M1
AE5 I2S3_MCLK_M0
AG4 I2S3_SCLK_M0_SOC — R1802 1 2 22R 5% R0402 — TP1800 TP_0.7 — I2S3_SCLK_M0
AF4 I2S3_LRCK_M0_SOC — R1803 1 2 22R 5% R0402 — I2S3_LRCK_M0
AH3 I2S3_SDO_M0 — TP1801 TP_0.7

AG3 I2S3_SDI_M0
AH2 GMAC1_INT/PMEB_GPIO3_A7
AG2 GMAC1_RSTn_GPIO3_B0

AG1 UART4_RX_M1
AF2 UART4_TX_M1
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AE2 RS485_DIR_GPIO3_B5
AE3 GPIO3_B6
AD4 GPIO3_B7
AD2 GPIO3_C0

AD1 PCIE20_PERSTn_M1
AA7 HP_DET_L_GPIO3_C2
AC4 SPK_CTL_H_GPIO3_C3

AC3 GPIO3_C4
AC2 GPIO3_C5

V10 VCCIO5_1
V11 VCCIO5_2

VCC_3V3
C1800 100nF X5R 10V C0201

VCC_3V3
R1800 10K 5% R0402 — R1801 10K 5% R0402
GMAC0_INT/PMEB_GPIO3_C0
GMAC1_INT/PMEB_GPIO3_A7
od

VCC_3V3
R1804 2.2K 5% R0402 — R1805 2.2K 5% R0402
I2C5_SCL_M0
I2C5_SDA_M0

If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID

Note:
If VCCIO5 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO5 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO5 will be abnormally.

The VCCIO5 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO5 will be damaged!

Default PCIe slot
GPIO3_B6 PCIE20_PRSNT_L_GPIO3_B6

PCIe Ethernet
GPIO3_B6 PCIE_ETH_ISOLATE_L_GPIO3_B6

QSGMII/SGMII
GPIO3_C4 GMAC1_MDC_M0
GPIO3_C5 GAMC1_MDIO_M0

Default UART7
GPIO3_C4 UART7_TX_M1
GPIO3_C5 UART7_RX_M1

Option

Default
GPIO3_B7 UART3_TX_M1
GPIO3_C0 UART3_RX_M1

GPIO3_B7 GMAC0_RSTn_GPIO3_B7
GPIO3_C0 GMAC0_INT/PMEB_GPIO3_C0

Option

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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Project:	RK3568_AIoT_REF_SCH			
File:	18.RK3568_VO Interface_2			
Date:	Wednesday, June 16, 2021		Rev:	V1.1
Designed by:	Zhangdz	Reviewed by: Default	Sheet:	19 of 72

RK3568_H(VCCIO1 Domain)

U1000H

VCCIO1 Domain

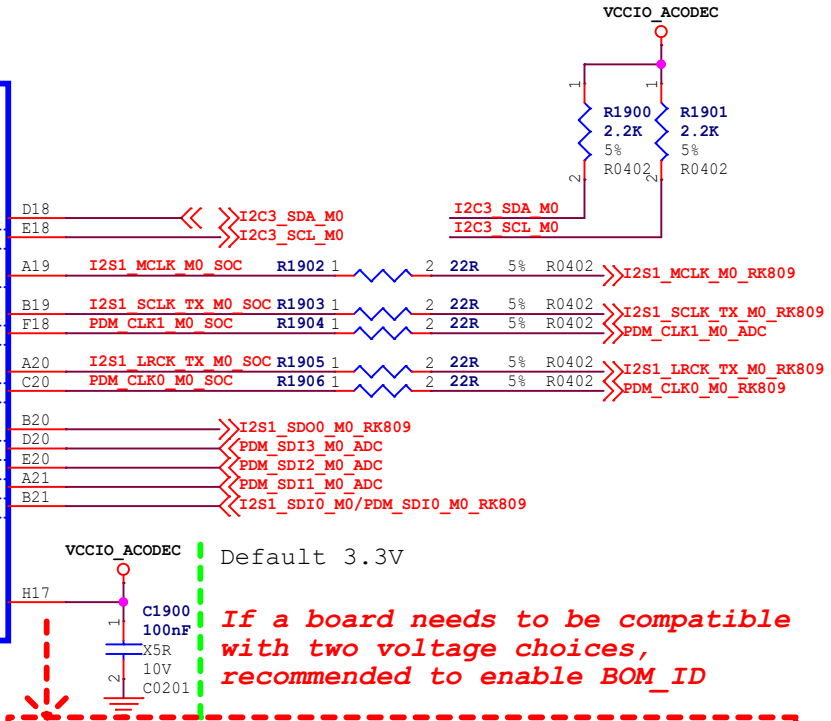
Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d

VCCIO1

RK3568

BGA636_19R00X19R00X1R20



Note:

If VCCIO1 domain power voltage is adjusted, the software DTS configuration must be updated synchronously, otherwise the IO may be damaged!

If the VCCIO1 hardware has been modified to 1.8V power supply, and the corresponding DTS must be modified to 1.8V configuration, otherwise the IO function of VCCIO1 will be abnormally.

The VCCIO1 hardware has been modified to 3.3V power supply, if the software DTS configuration is still 1.8V configuration, the IO of VCCIO1 will be damaged!

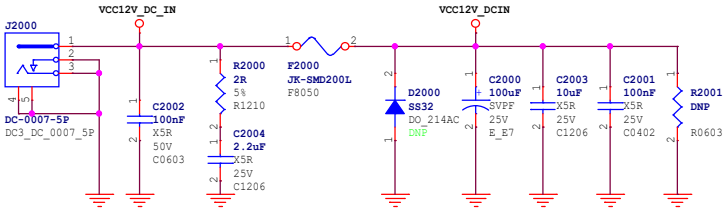
Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

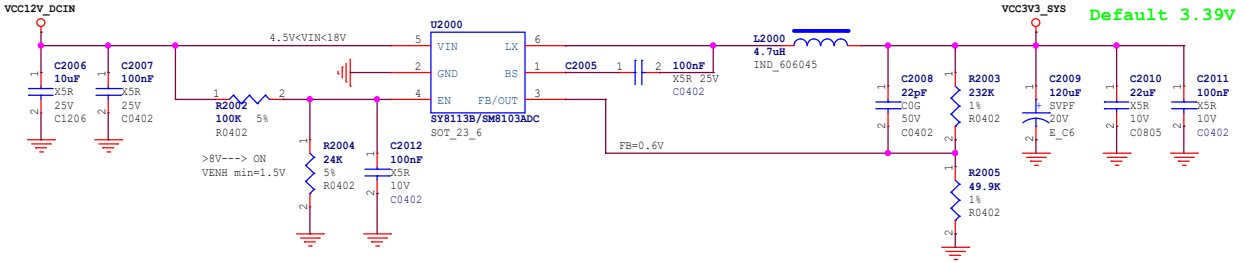
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	19.RK3568_Audio Interface				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	20 of 72

12V/3A DCIN

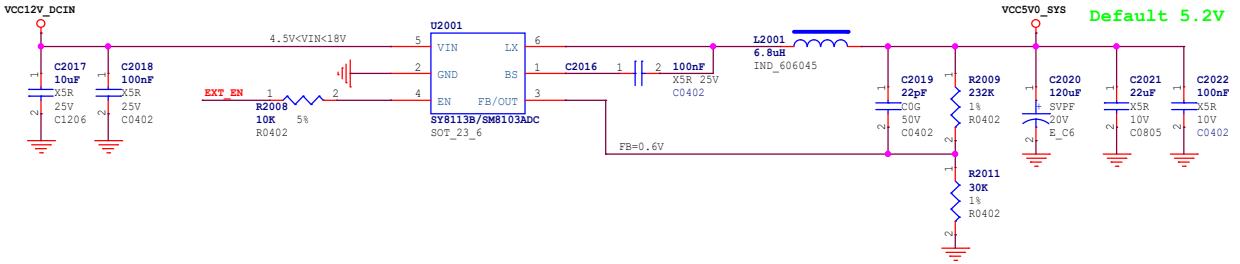
Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe

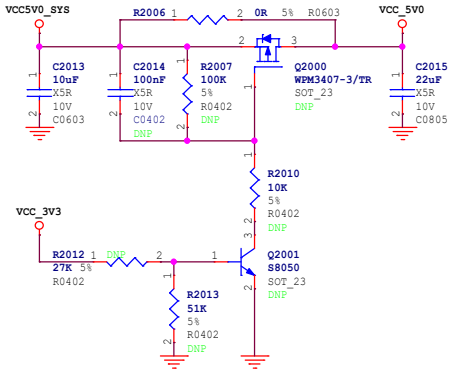


VCC3V3_SYS

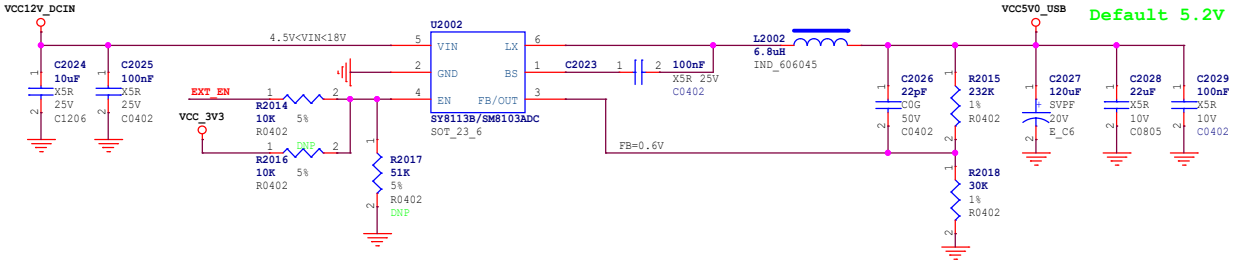


VCC5V0_SYS





VCC5V0_USB



EXT_EN

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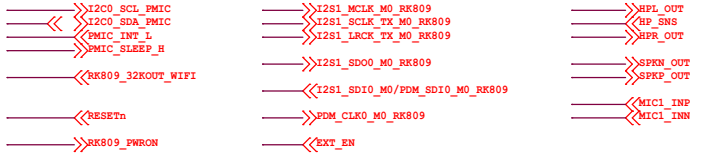
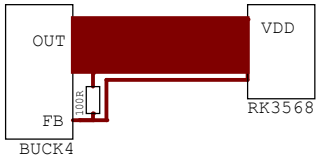
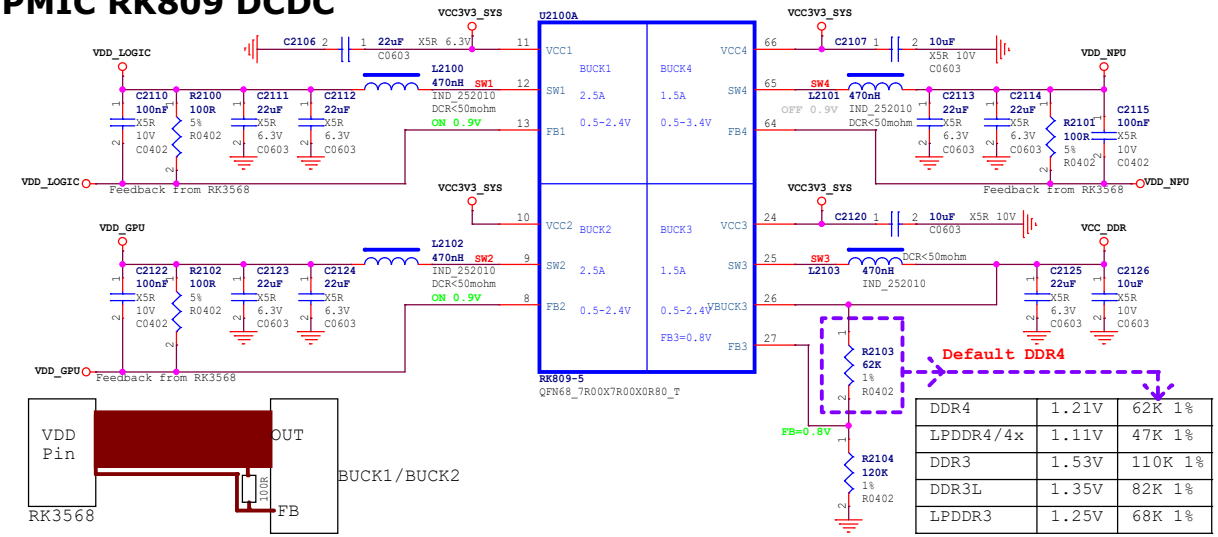
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	20.Power_DC IN				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	21 of 72



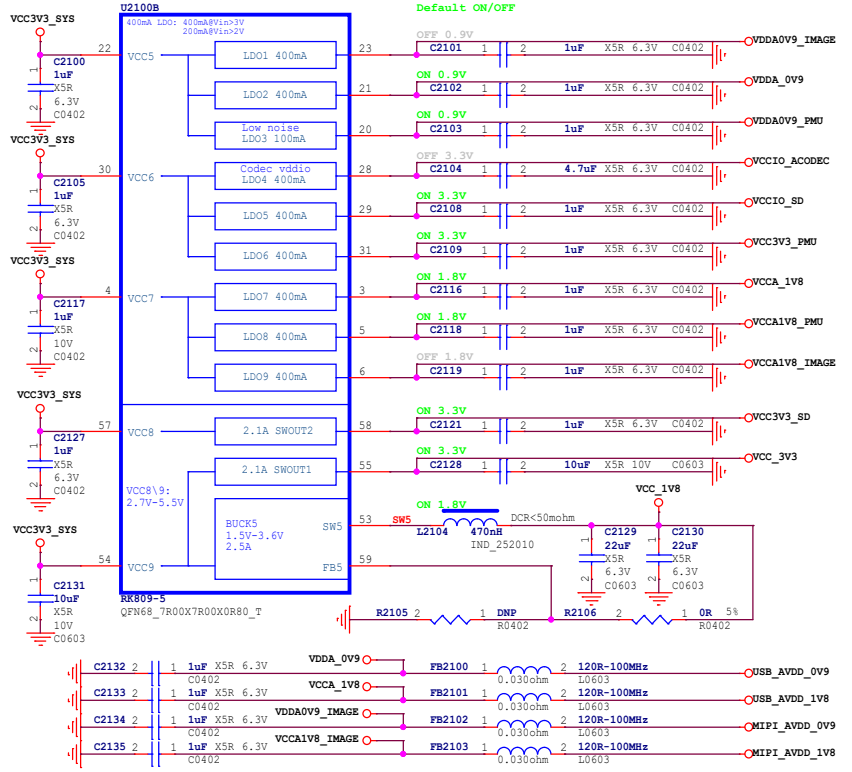


PMIC RK809 DCDC

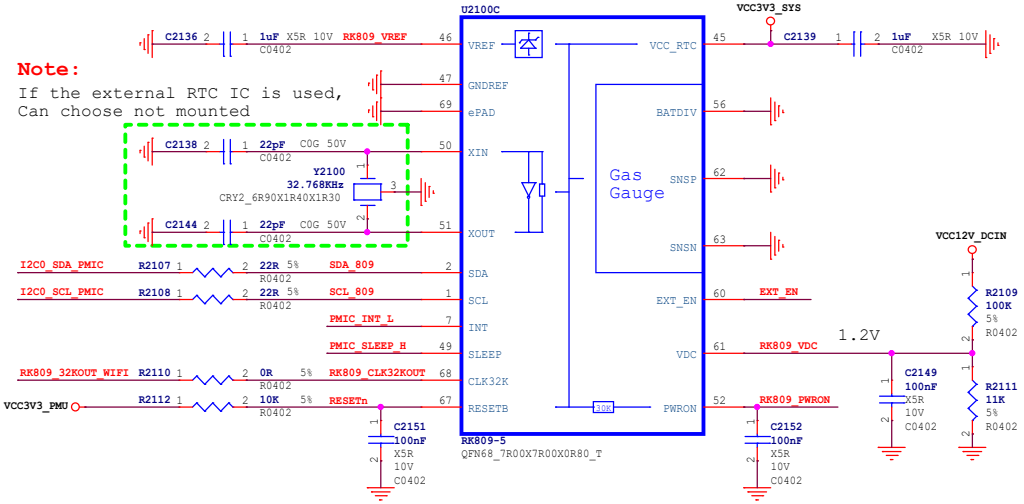


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

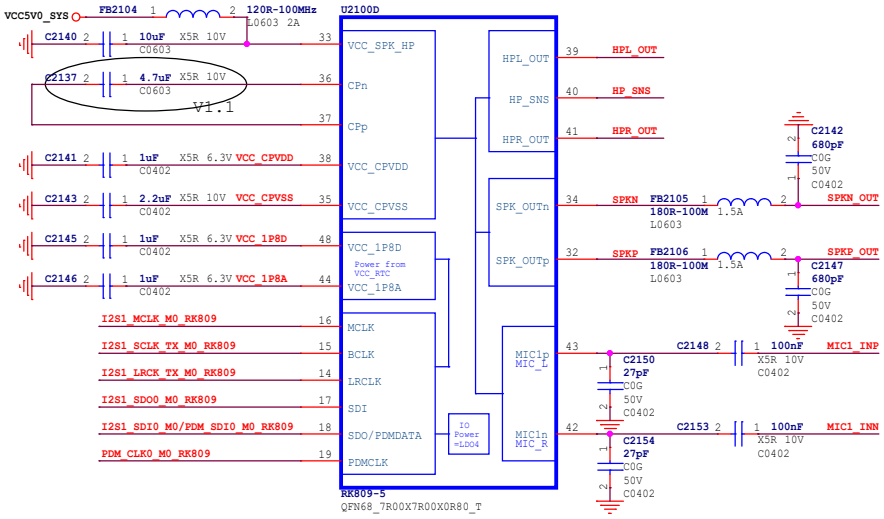
PMIC RK809 LDO



PMIC RK809 Management



PMIC RK809 CODEC



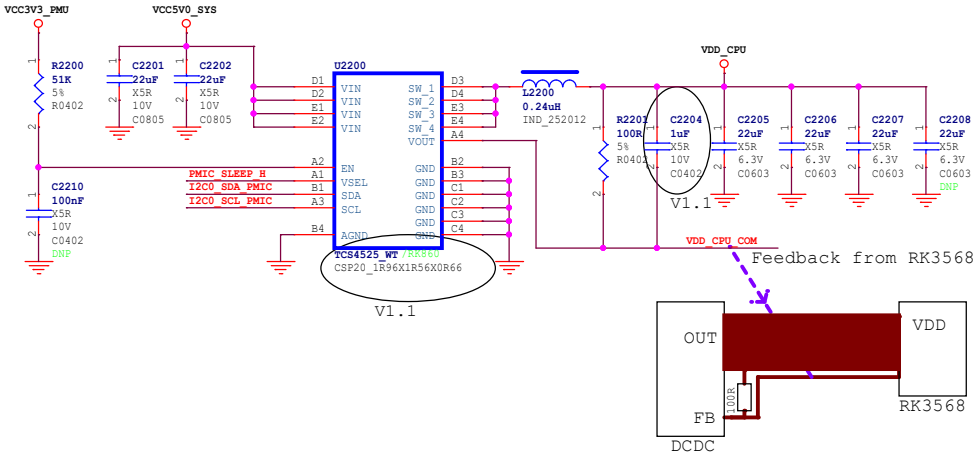
Note:

If RK809-5 codec is not used,
then Pin 14,15,16,17,19,40 Tie VSS
Pin 18,36,37,38,35,39,41,34,32,43,42
Leave floating

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	21.Power_PMIC				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 72

I2C0_SCL_PMIC
I2C0_SDA_PMIC
PMIC_SLEEP_H
VDD_CPU_COM
RTCIC_INT_L_GPIO0_D3
RTCIC_32KOUT
I2C5_SCL_M0
I2C5_SDA_M0
LCD0_PWREN_H_GPIO0_C7
LCD1_PWREN_H_GPIO0_C5

VDD_CPU

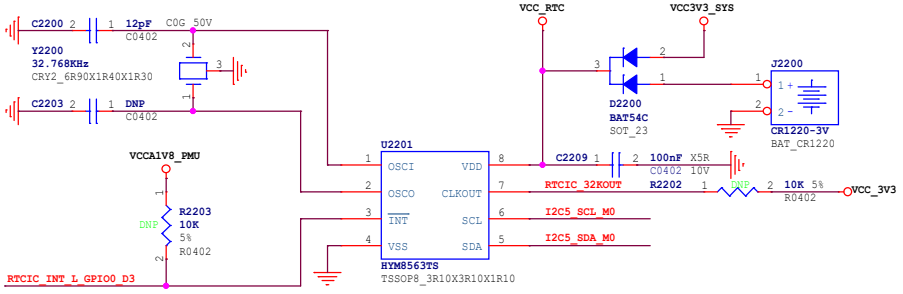


RTC IC --Option

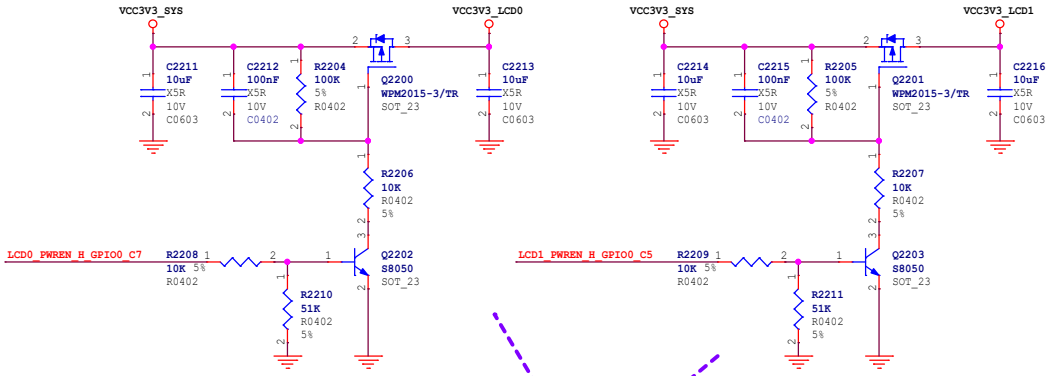
Note:

The power off hold time scheme is required,
It is recommended to use external RTC IC

But, it will not support the timing poweron function



Address:Read A3H,Write A2H



According to the actual product assigned to the LCM

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	22.Power_Ext Discrete/RTC IC				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	23 of 72

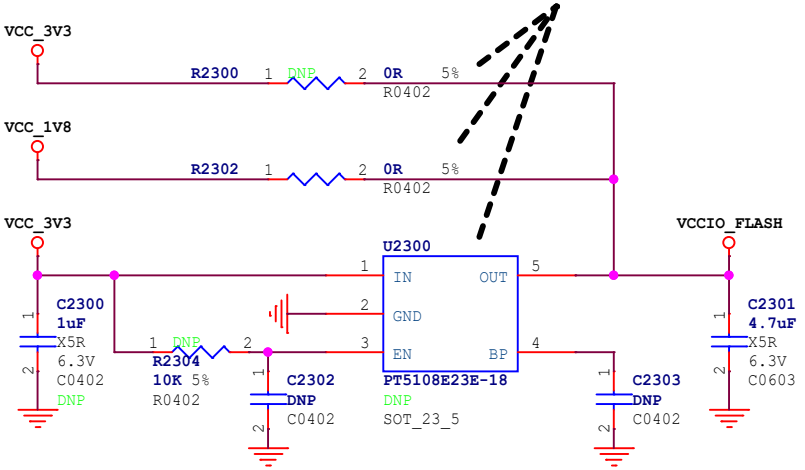
FLASH_VOL_SEL

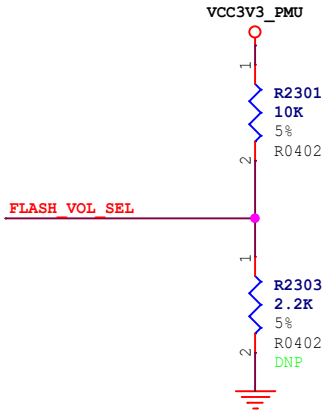
Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Optional 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 1.8V, Optional 3.3V	FLASH_VOL_SEL --> Logic=H(Default)

Note:

According to the actual choice of mounted
Cannot be mounted at the same time

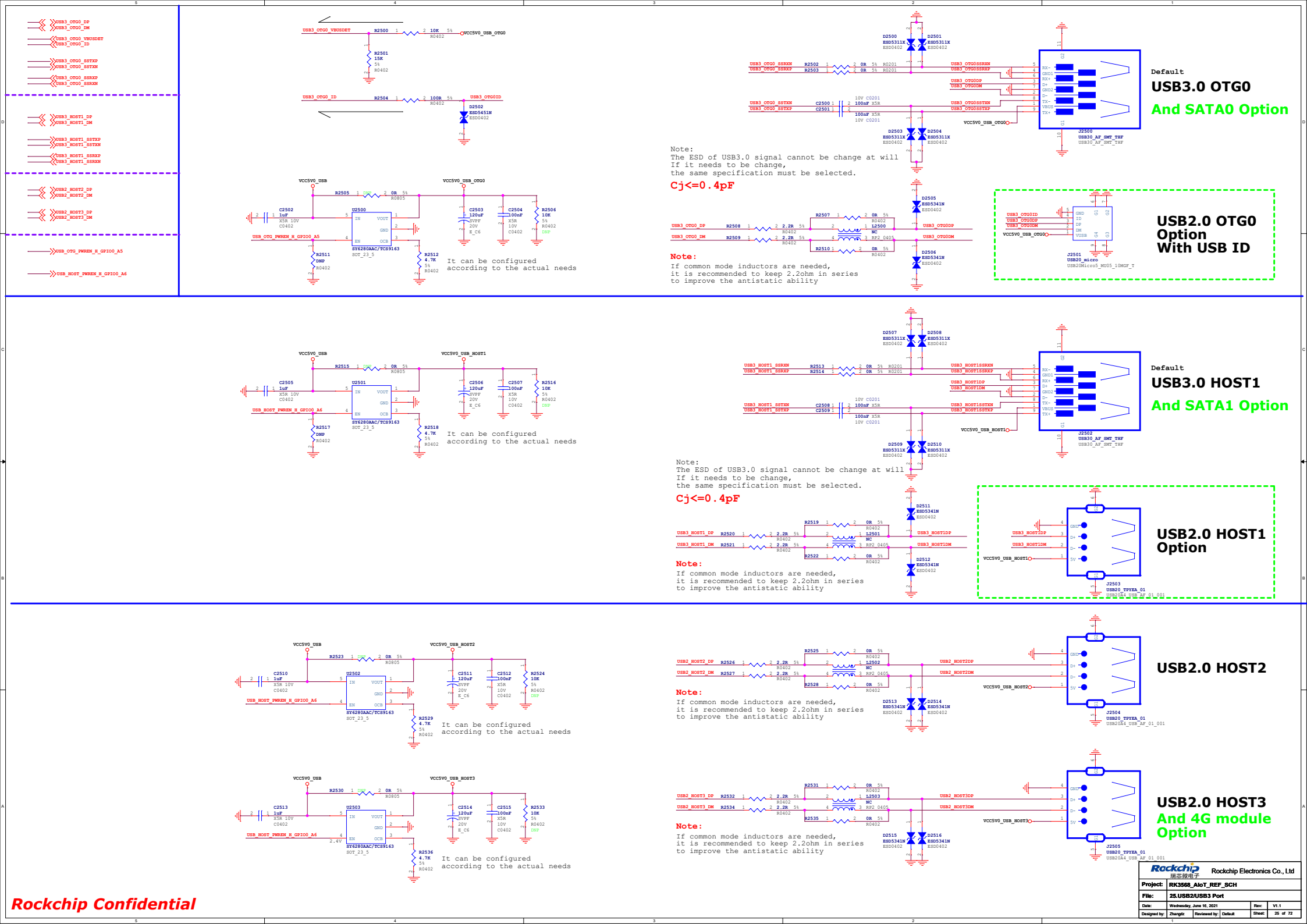




Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

When VCCIO2 voltage is connected to 1.8V, FLASH_VOL_SEL must be high
When VCCIO2 voltage is connected to 3.3V, FLASH_VOL_SEL must be low
If VCCIO2 power supply voltage and FLASH_VOL_SEL fails to meet the above relationship,
its function will be abnormally(for example, it cannot be started normally) or IO will be damaged.

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	23.Power_Flash Power Manage				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	24 of 72


USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB3_OTG0_ID
USB3_OTG0_SSTXP
USB3_OTG0_SSTXN
USB3_OTG0_SSRXP
USB3_OTG0_SSRXN
USB3_HOST1_DP
USB3_HOST1_DM
USB3_HOST1_SSTXP
USB3_HOST1_SSTXN
USB3_HOST1_SSRXP
USB3_HOST1_SSRXN
USB2_HOST2_DP
USB2_HOST2_DM
USB2_HOST3_DP
USB2_HOST3_DM
USB_OTG_PWREN_H_GPIO0_A5
USB_HOST_PWREN_H_GPIO0_A6
USB3_OTG0_VBUSDET
R2500 10K 5% R0402
VCC5V0_USB_OTG0
R2501 15K 5% R0402
USB3_OTG0_ID
R2504 100R 5% R0402
USB3_OTG0ID
D2502 ESD5451N ESD0402
VCC5V0_USB
VCC5V0_USB_OTG0
R2505 0R 5% R0805 DNP
C2502 1uF X5R 10V C0402
U2500 SY6280AAC/TCS9163 SOT_23_5
C2503 120uF SVPF 20V E_C6
C2504 100nF X5R 10V C0402
R2506 10K 5% R0402 DNP
R2511 DNP R0402
R2512 4.7K 5% R0402
It can be configured according to the actual needs
D2500 D2501 ESD5311X ESD0402
USB3_OTG0_SSRXN USB3_OTG0_SSRXP R2502 R2503 0R 5% R0201
USB3_OTG0SSRXN USB3_OTG0SSRXP
USB3_OTG0DP USB3_OTG0DM
USB3_OTG0_SSTXN USB3_OTG0_SSTXP C2500 C2501 100nF X5R 10V C0201
USB3_OTG0SSTXN USB3_OTG0SSTXP
D2503 D2504 ESD5311X ESD0402
J2500 USB30_AF_SMT_THF
Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.
Cj<=0.4pF
Default
USB3.0 OTG0
And SATA0 Option
D2505 ESD5341N ESD0402
USB3_OTG0_DP USB3_OTG0_DM R2508 R2509 2.2R 5% R0402
R2507 0R R0402 NC
L2500 RP2_0405
USB3_OTG0DP USB3_OTG0DM
R2510 0R 5% R0402
D2506 ESD5341N ESD0402
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
USB3_OTG0ID USB3_OTG0DP USB3_OTG0DM VCC5V0_USB_OTG0
J2501 USB20_micro USB20Micro5_MU05_10MGF_T
USB2.0 OTG0 Option With USB ID
VCC5V0_USB
VCC5V0_USB_HOST1
R2515 0R 5% R0805 DNP
C2505 1uF X5R 10V C0402
U2501 SY6280AAC/TCS9163 SOT_23_5
C2506 120uF SVPF 20V E_C6
C2507 100nF X5R 10V C0402
R2516 10K 5% R0402 DNP
USB_HOST_PWREN_H_GPIO0_A6
R2517 DNP R0402
R2518 4.7K 5% R0402
It can be configured according to the actual needs
D2507 D2508 ESD5311X ESD0402
USB3_HOST1_SSRXN USB3_HOST1_SSRXP R2513 R2514 0R 5% R0201
USB3_HOST1SSRXN USB3_HOST1SSRXP
USB3_HOST1DP USB3_HOST1DM
USB3_HOST1_SSTXN USB3_HOST1_SSTXP C2508 C2509 100nF X5R 10V C0201
USB3_HOST1SSTXN USB3_HOST1SSTXP
D2509 D2510 ESD5311X ESD0402
J2502 USB30_AF_SMT_THF
Note:
The ESD of USB3.0 signal cannot be change at will
If it needs to be change,
the same specification must be selected.
Cj<=0.4pF
Default
USB3.0 HOST1
And SATA1 Option
D2511 ESD5341N ESD0402
USB3_HOST1_DP USB3_HOST1_DM R2519 R2520 R2521 2.2R 5% R0402
R2522 0R 5% R0402
L2501 NC RP2_0405
USB3_HOST1DP USB3_HOST1DM
D2512 ESD5341N ESD0402
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
VCC5V0_USB_HOST1
J2503 USB20_TPYEA_01 USB20A4_USB_AF_01_001
USB2.0 HOST1 Option
VCC5V0_USB
VCC5V0_USB_HOST2
R2523 0R 5% R0805 DNP
C2510 1uF X5R 10V C0402
U2502 SY6280AAC/TCS9163 SOT_23_5
C2511 120uF SVPF 20V E_C6
C2512 100nF X5R 10V C0402
R2524 10K 5% R0402 DNP
USB_HOST_PWREN_H_GPIO0_A6
R2529 4.7K 5% R0402
It can be configured according to the actual needs
D2513 D2514 ESD5341N ESD0402
USB2_HOST2_DP USB2_HOST2_DM R2526 R2527 2.2R 5% R0402
R2525 0R 5% R0402
L2502 NC RP2_0405
R2528 0R 5% R0402
USB2_HOST2DP USB2_HOST2DM
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
VCC5V0_USB_HOST2
J2504 USB20_TPYEA_01 USB20A4_USB_AF_01_001
USB2.0 HOST2
VCC5V0_USB
VCC5V0_USB_HOST3
R2530 0R 5% R0805 DNP
C2513 1uF X5R 10V C0402
U2503 SY6280AAC/TCS9163 SOT_23_5
C2514 120uF SVPF 20V E_C6
C2515 100nF X5R 10V C0402
R2533 10K 5% R0402 DNP
USB_HOST_PWREN_H_GPIO0_A6
R2536 4.7K 5% R0402
It can be configured according to the actual needs
D2515 D2516 ESD5341N ESD0402
USB2_HOST3_DP USB2_HOST3_DM R2532 R2534 2.2R 5% R0402
R2531 0R 5% R0402
L2503 NC RP2_0405
R2535 0R 5% R0402
USB2_HOST3DP USB2_HOST3DM
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
VCC5V0_USB_HOST3
J2505 USB20_TPYEA_01 USB20A4_USB_AF_01_001
USB2.0 HOST3
And 4G module
Option
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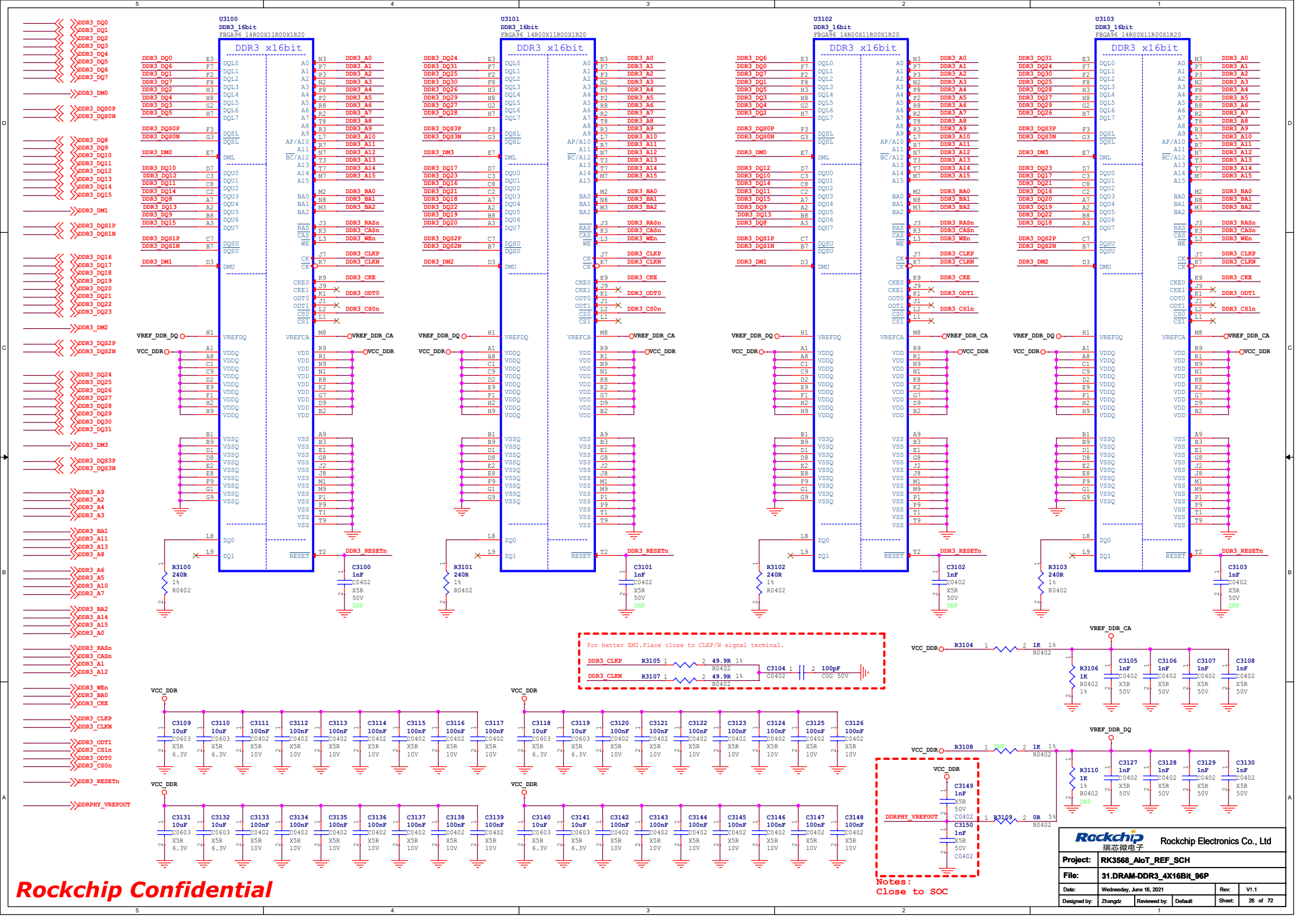
Rockchip Electronics Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 25.USB2/USB3 Port
Date: Wednesday, June 16, 2021
Rev: V1.1
Designed by: Zhangtz
Reviewed by: Default
Sheet: 25 of 72


U3100
DDR3_16bit
FBGA96_14R00X11R00X1R20
DDR3 x16bit
U3101
DDR3_16bit
FBGA96_14R00X11R00X1R20
DDR3 x16bit
U3102
DDR3_16bit
FBGA96_14R00X11R00X1R20
DDR3 x16bit
U3103
DDR3_16bit
FBGA96_14R00X11R00X1R20
DDR3 x16bit
DDR3_DQ0
DDR3_DQ1
DDR3_DQ2
DDR3_DQ3
DDR3_DQ4
DDR3_DQ5
DDR3_DQ6
DDR3_DQ7
DDR3_DM0
DDR3_DQS0P
DDR3_DQS0N
DDR3_DQ8
DDR3_DQ9
DDR3_DQ10
DDR3_DQ11
DDR3_DQ12
DDR3_DQ13
DDR3_DQ14
DDR3_DQ15
DDR3_DM1
DDR3_DQS1P
DDR3_DQS1N
DDR3_DQ16
DDR3_DQ17
DDR3_DQ18
DDR3_DQ19
DDR3_DQ20
DDR3_DQ21
DDR3_DQ22
DDR3_DQ23
DDR3_DM2
DDR3_DQS2P
DDR3_DQS2N
DDR3_DQ24
DDR3_DQ25
DDR3_DQ26
DDR3_DQ27
DDR3_DQ28
DDR3_DQ29
DDR3_DQ30
DDR3_DQ31
DDR3_DM3
DDR3_DQS3P
DDR3_DQS3N
DDR3_A9
DDR3_A2
DDR3_A4
DDR3_A3
DDR3_BA1
DDR3_A11
DDR3_A13
DDR3_A8
DDR3_A6
DDR3_A5
DDR3_A10
DDR3_A7
DDR3_BA2
DDR3_A14
DDR3_A15
DDR3_A0
DDR3_RASn
DDR3_CASn
DDR3_A1
DDR3_A12
DDR3_WEn
DDR3_BA0
DDR3_CKE
DDR3_CLKP
DDR3_CLKN
DDR3_ODT1
DDR3_CS1n
DDR3_ODT0
DDR3_CS0n
DDR3_RESETn
DDRPHY_VREFOUT
VREF_DDR_DQ
VREF_DDR_CA
VCC_DDR
R3100 240R 1% R0402
R3101 240R 1% R0402
R3102 240R 1% R0402
R3103 240R 1% R0402
C3100 1nF C0402 X5R 50V DNP
C3101 1nF C0402 X5R 50V DNP
C3102 1nF C0402 X5R 50V DNP
C3103 1nF C0402 X5R 50V DNP
For better EMI.Place close to CLKP/N signal terminal.
DDR3_CLKP
DDR3_CLKN
R3105 49.9R 1% R0402
R3107 49.9R 1% R0402
C3104 100pF C0G 50V
R3104 1K 1% R0402
R3106 1K 1% R0402
C3105 1nF C0402 X5R 50V
C3106 1nF C0402 X5R 50V
C3107 1nF C0402 X5R 50V
C3108 1nF C0402 X5R 50V
R3108 1K 1% R0402 DNP
R3110 1K 1% R0402 DNP
C3127 1nF C0402 X5R 50V
C3128 1nF C0402 X5R 50V
C3129 1nF C0402 X5R 50V
C3130 1nF C0402 X5R 50V
C3109 10uF C0603 X5R 6.3V
C3110 10uF C0603 X5R 6.3V
C3111 100nF C0402 X5R 10V
C3112 100nF C0402 X5R 10V
C3113 100nF C0402 X5R 10V
C3114 100nF C0402 X5R 10V
C3115 100nF C0402 X5R 10V
C3116 100nF C0402 X5R 10V
C3117 100nF C0402 X5R 10V
C3118 10uF C0603 X5R 6.3V
C3119 10uF C0603 X5R 6.3V
C3120 100nF C0402 X5R 10V
C3121 100nF C0402 X5R 10V
C3122 100nF C0402 X5R 10V
C3123 100nF C0402 X5R 10V
C3124 100nF C0402 X5R 10V
C3125 100nF C0402 X5R 10V
C3126 100nF C0402 X5R 10V
C3131 10uF C0603 X5R 6.3V
C3132 10uF C0603 X5R 6.3V
C3133 100nF C0402 X5R 10V
C3134 100nF C0402 X5R 10V
C3135 100nF C0402 X5R 10V
C3136 100nF C0402 X5R 10V
C3137 100nF C0402 X5R 10V
C3138 100nF C0402 X5R 10V
C3139 100nF C0402 X5R 10V
C3140 10uF C0603 X5R 6.3V
C3141 10uF C0603 X5R 6.3V
C3142 100nF C0402 X5R 10V
C3143 100nF C0402 X5R 10V
C3144 100nF C0402 X5R 10V
C3145 100nF C0402 X5R 10V
C3146 100nF C0402 X5R 10V
C3147 100nF C0402 X5R 10V
C3148 100nF C0402 X5R 10V
C3149 1nF C0402 X5R 50V
C3150 1nF C0402 X5R 50V
R3109 0R 5% R0402
Notes:
Close to SOC
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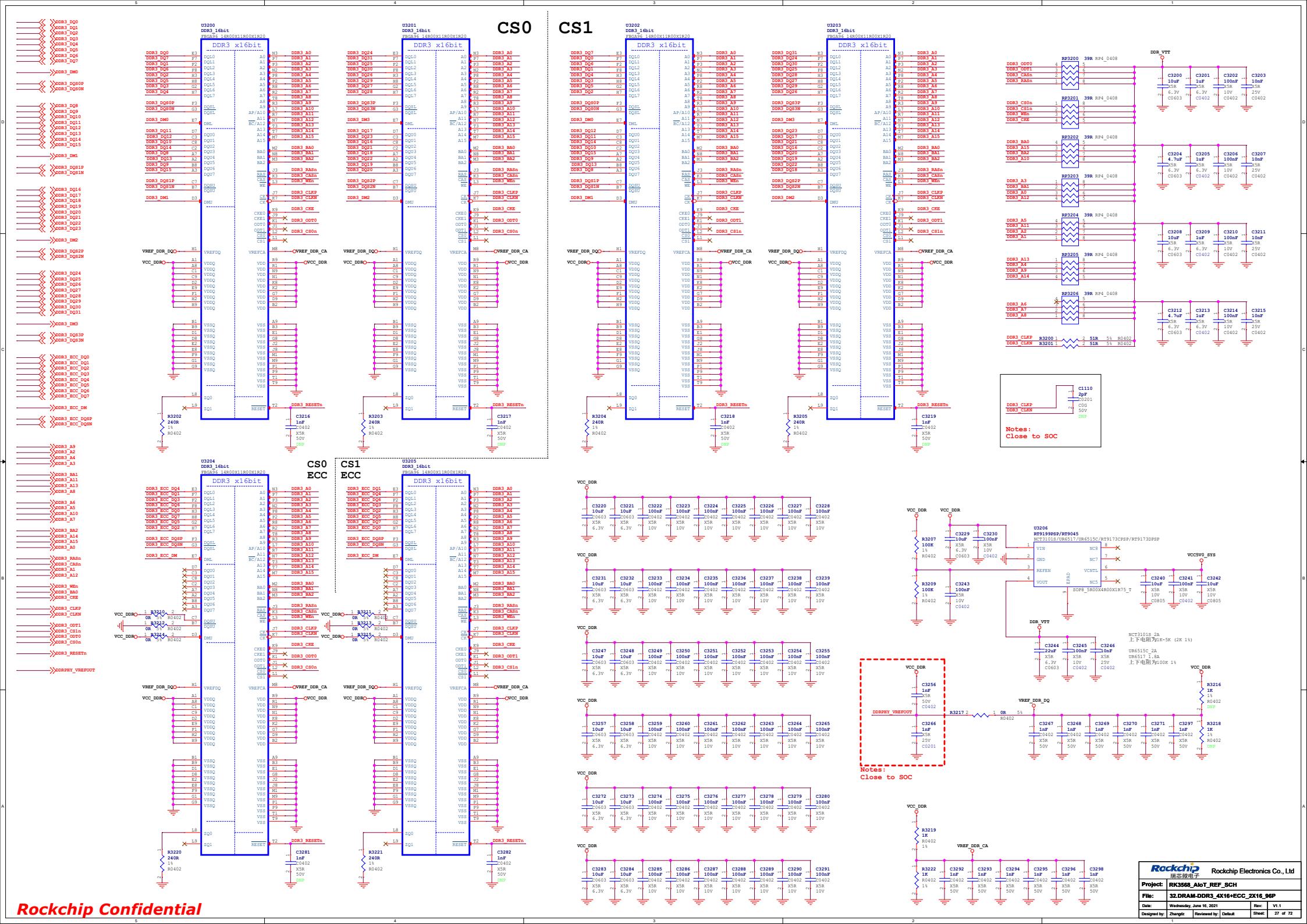
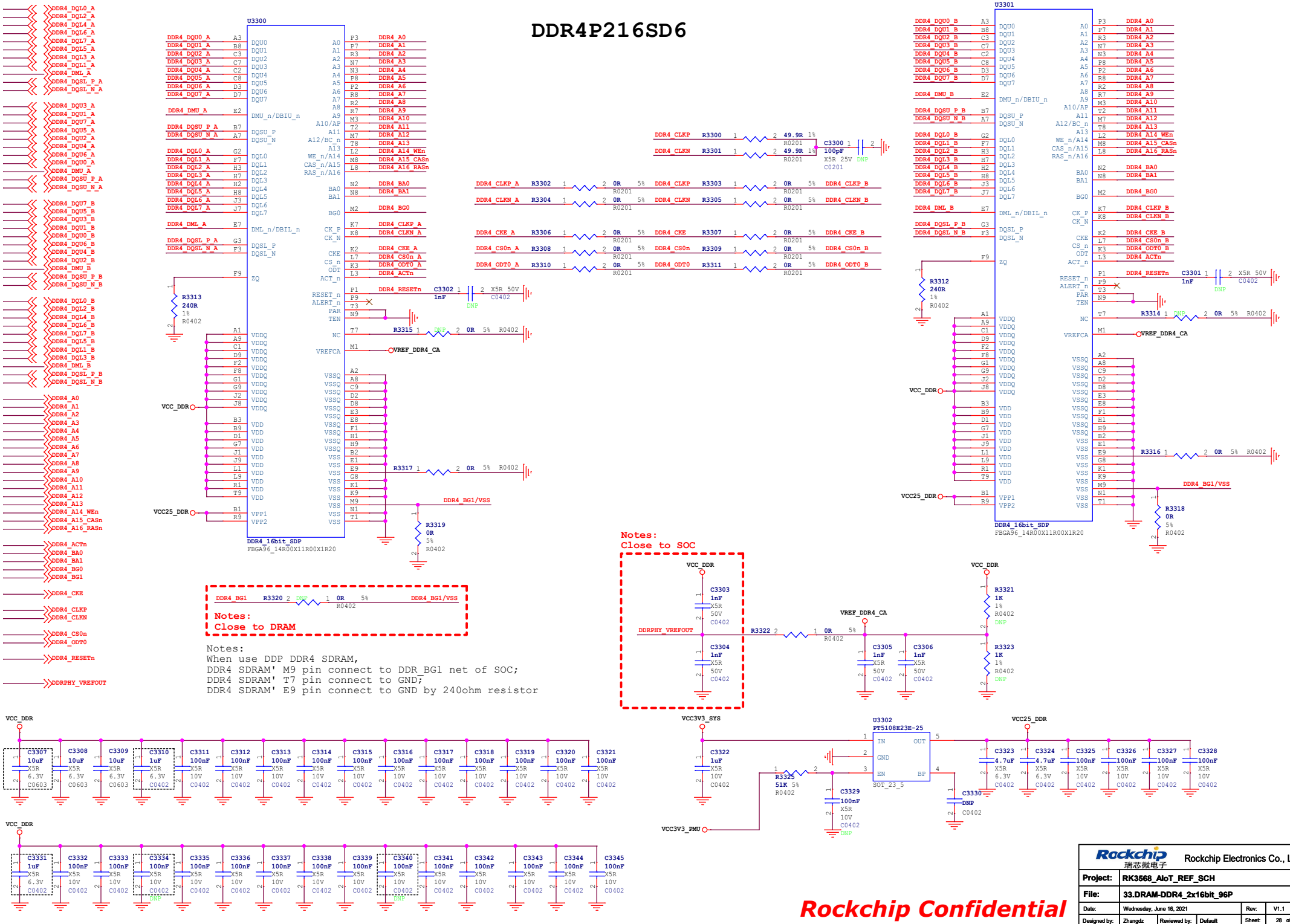
Project: RK3568_AIoT_REF_SCH
File: 31.DRAM-DDR3_4X16Bit_96P
Date: Wednesday, June 16, 2021
Rev: V1.1
Designed by: Zhangdz
Reviewed by: Default
Sheet: 26 of 72

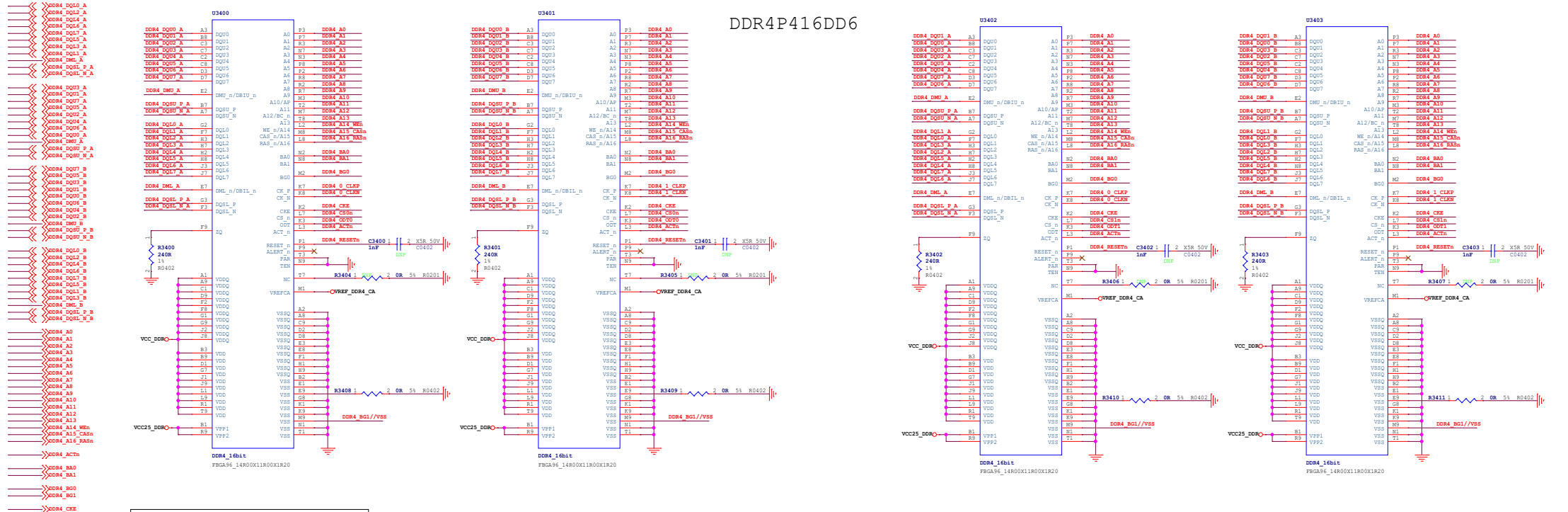

CS0
CS1
CS0 ECC
CS1 ECC
DDR3 x16bit
Notes:
Close to SOC
Notes:
Close to SOC
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 32.DRAM-DDR3_4X16+ECC_2X16_96P
Date: Wednesday, June 16, 2021
Rev: V1.1
Designed by: Zhangtz
Reviewed by: Default
Sheet: 27 of 72

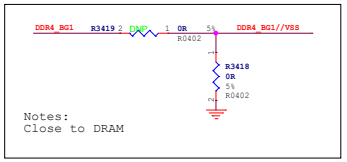
DDR4P216SD6



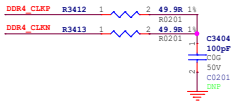
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	33.DRAM-DDR4_2x16bit_96P				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	28 of 72

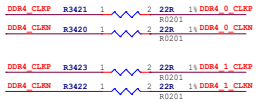
DDR4P416DD6

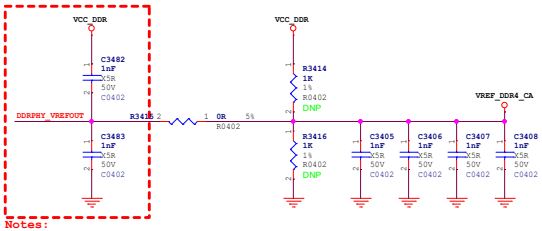


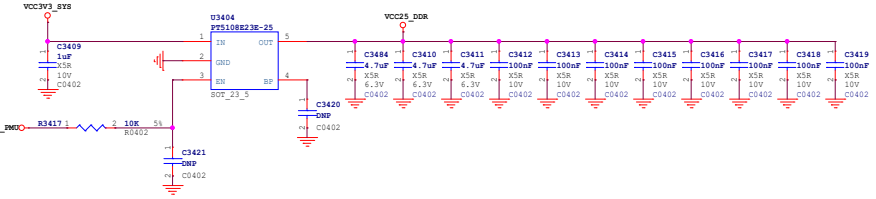


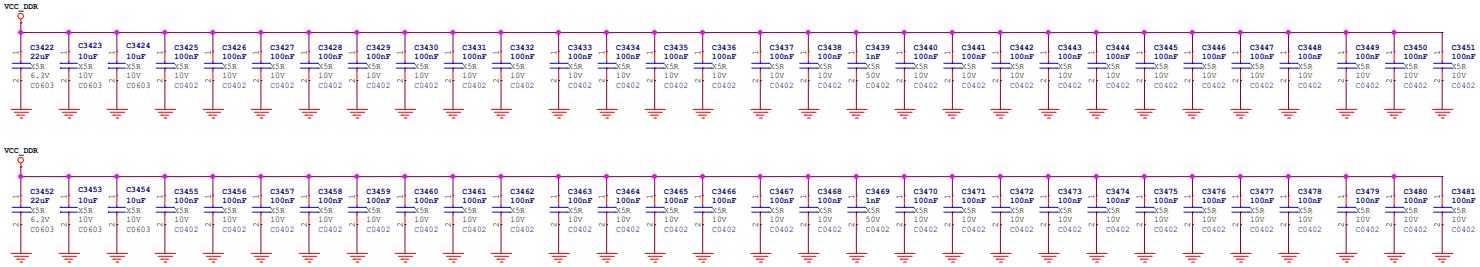
Notes:
When use 16Gbit/32Gbit DDR4 SDRAM,
DDR4 SDRAM' M9 pin connect to DDR_BG1 net of SOC;
DDR4 SDRAM' T7 pin connect to GND;
DDR4 SDRAM' E9 pin connect to GND by 240ohm resistor



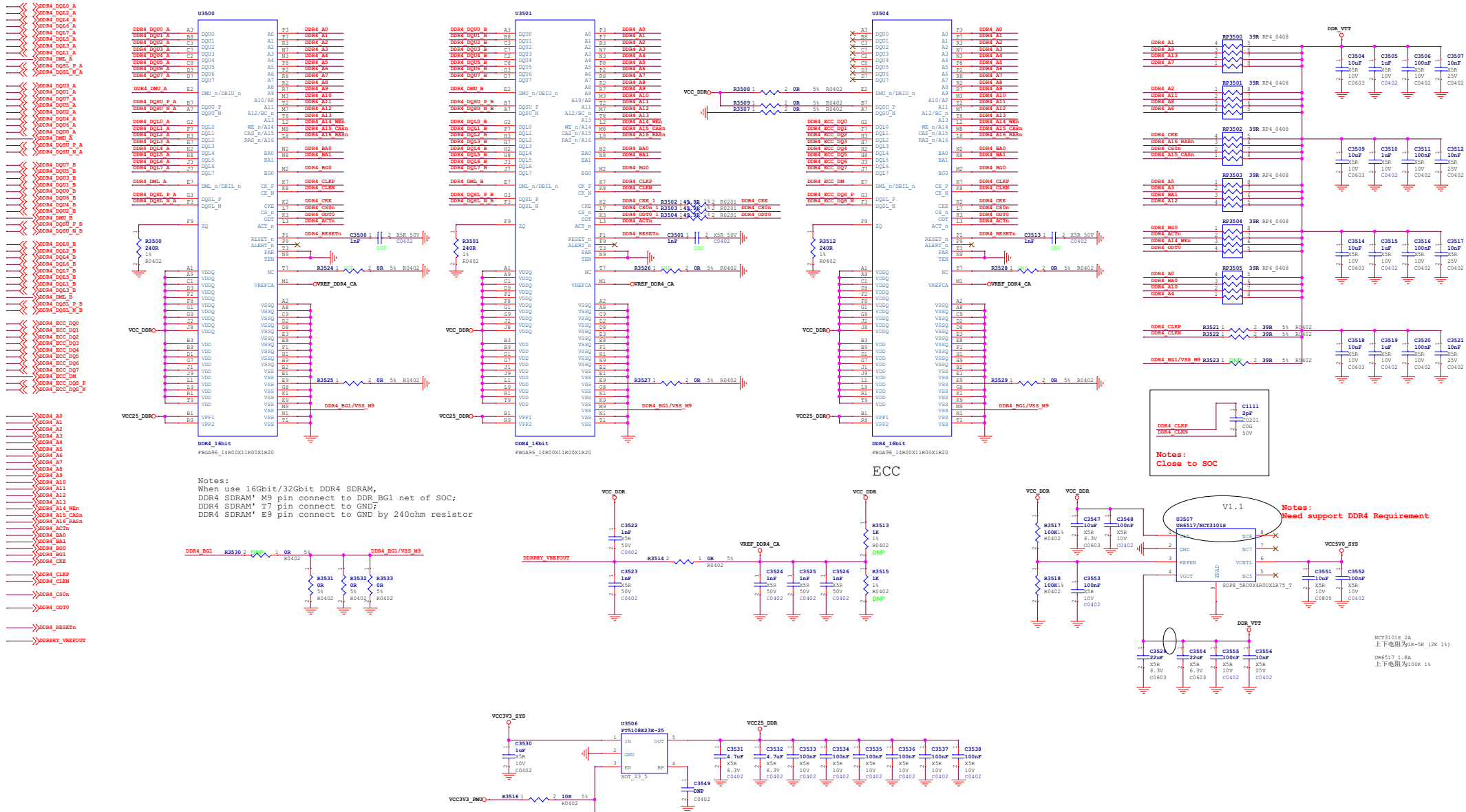




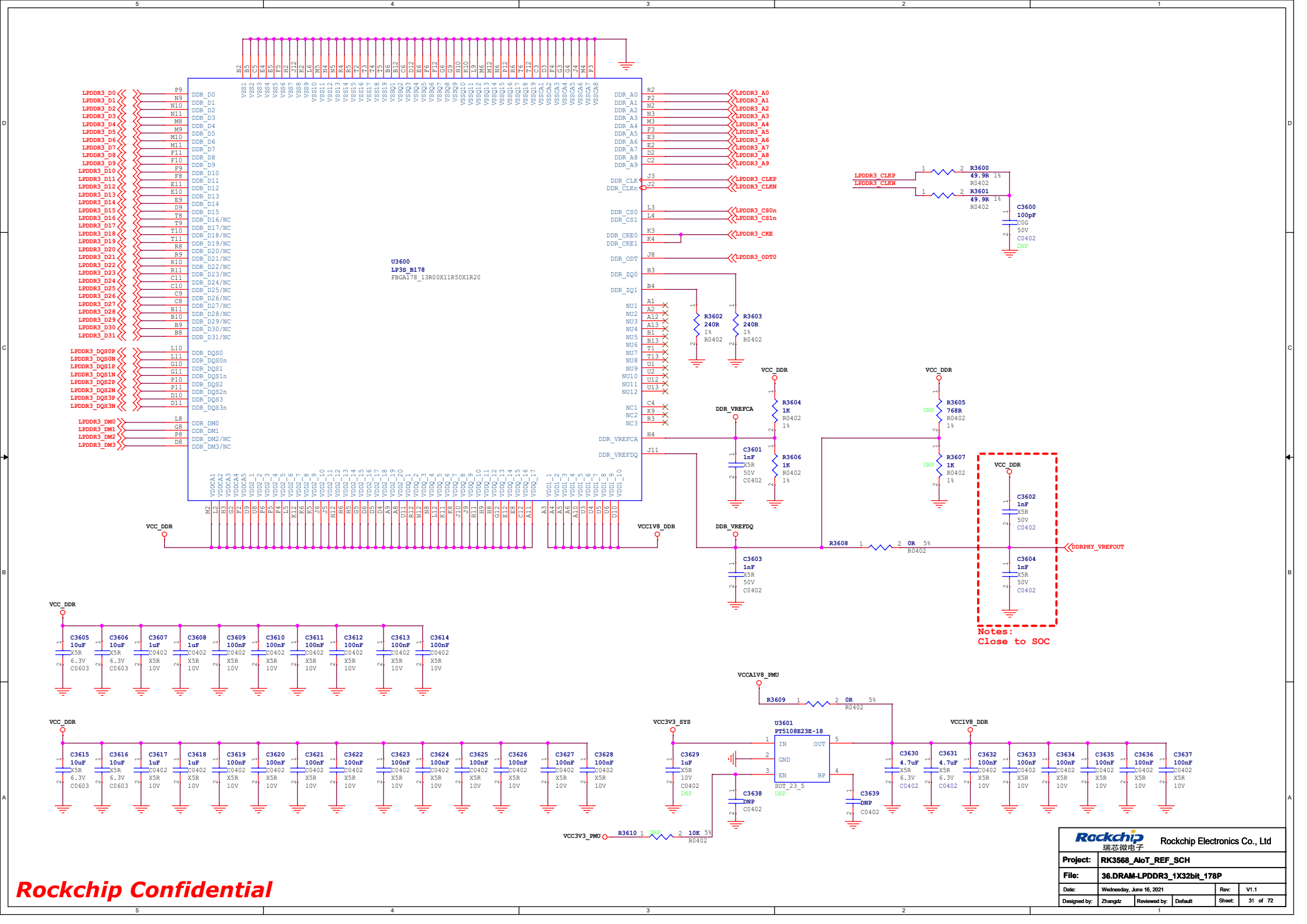




Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	34.DRAM-DDR4_4x16Bit_96P		
Date:	Wednesday, June 16, 2021	Rev:	V1.1
Designed by: Zhangtz	Reviewed by: Default	Sheet:	29 of 72

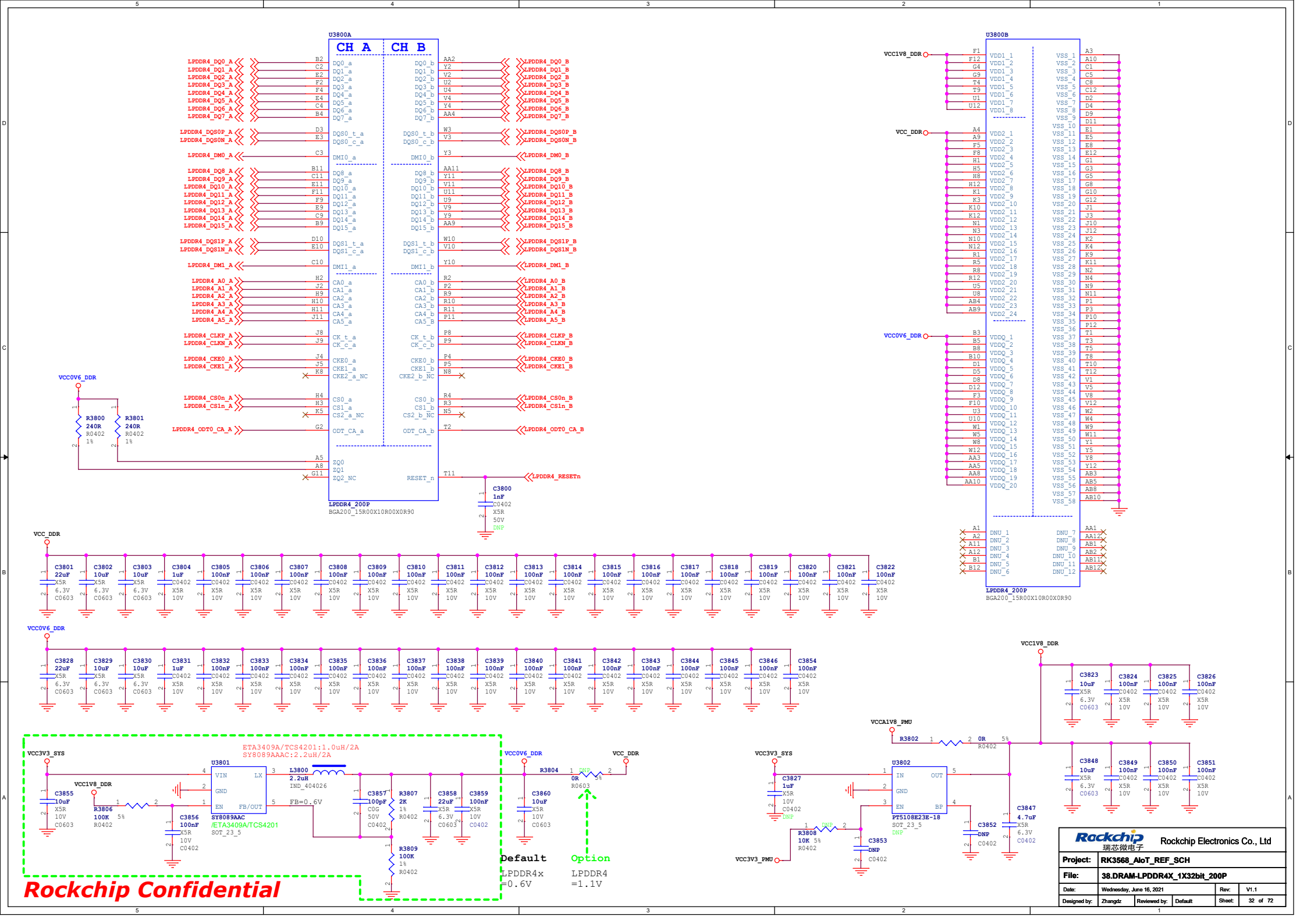


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	35.DRAM-DDR4_96P_2X16+ECC_1X16
Date:	Wednesday, June 16, 2021
Rev:	V1.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	30 of 72

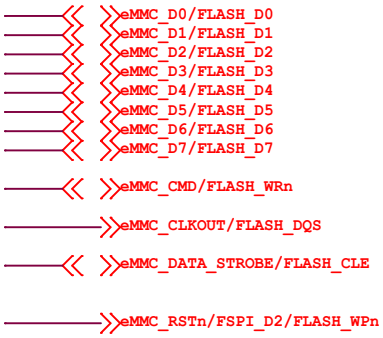


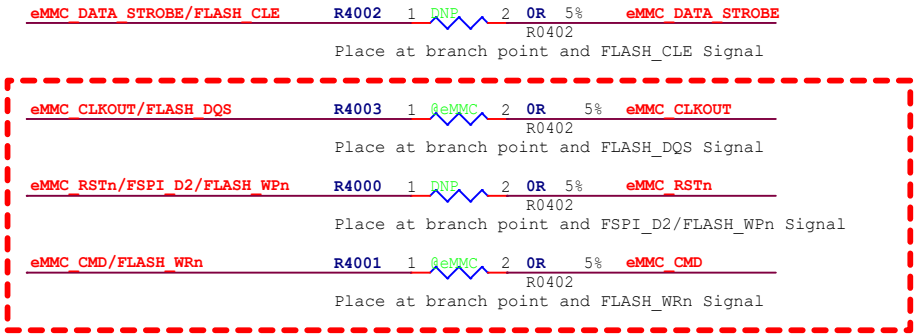
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3568_AIoT_REF_SCH				
File:	36.DRAM-LPDDR3_1X32bit_178P				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	31 of 72


U3800A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U3800B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VCC_DDR
VCC0V6_DDR
VCC1V8_DDR
VCCA1V8_PMU
VCC3V3_SYS
VCC3V3_PMU
R3800 240R R0402 1%
R3801 240R R0402 1%
C3800 1nF C0402 X5R 50V DNP
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
U3801
SY8089AAC
/ETA3409A/TCS4201
SOT_23_5
L3800 2.2uH IND_404026
FB=0.6V
R3804 0R R0603 DNP
Default
LPDDR4x
=0.6V
Option
LPDDR4
=1.1V
U3802
PT5108E23E-18
SOT_23_5
Rockchip Confidential
Rockchip Electronics Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 38.DRAM-LPDDR4X_1X32bit_200P
Date: Wednesday, June 16, 2021
Rev: V1.1
Designed by: Zhangdz
Reviewed by: Default
Sheet: 32 of 72

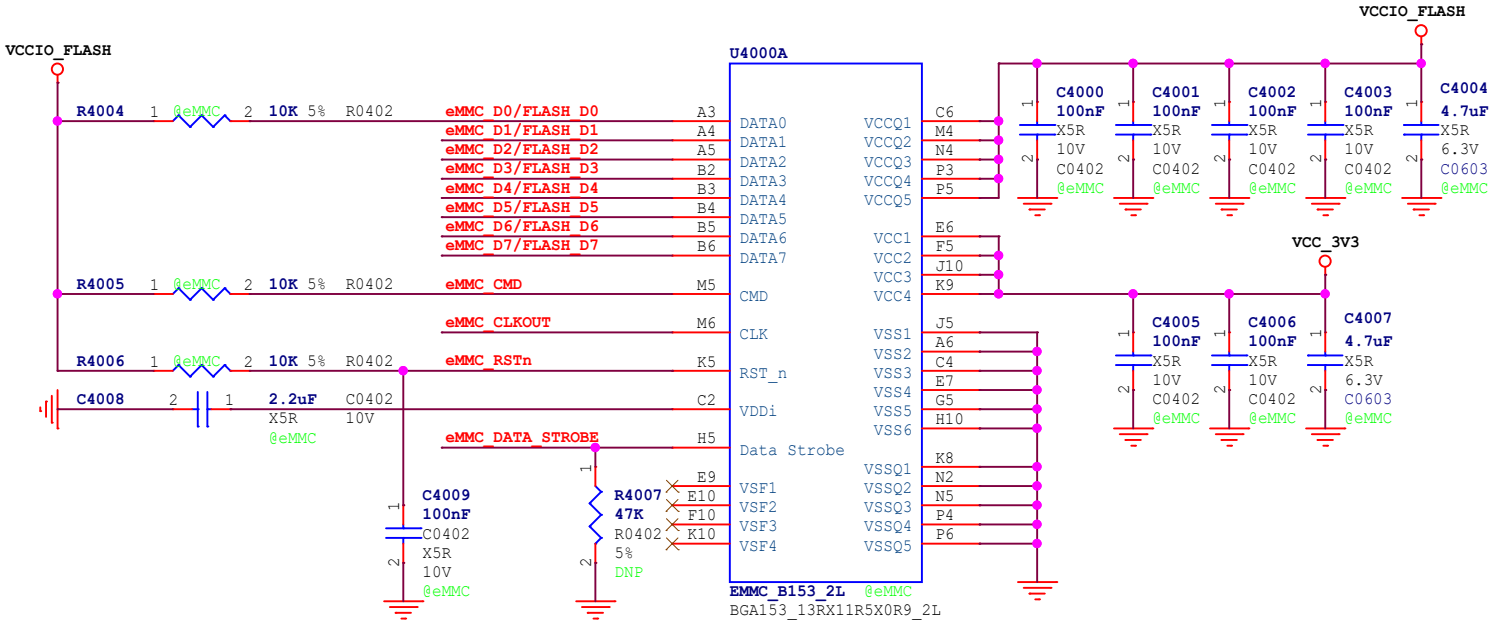
eMMC Flash

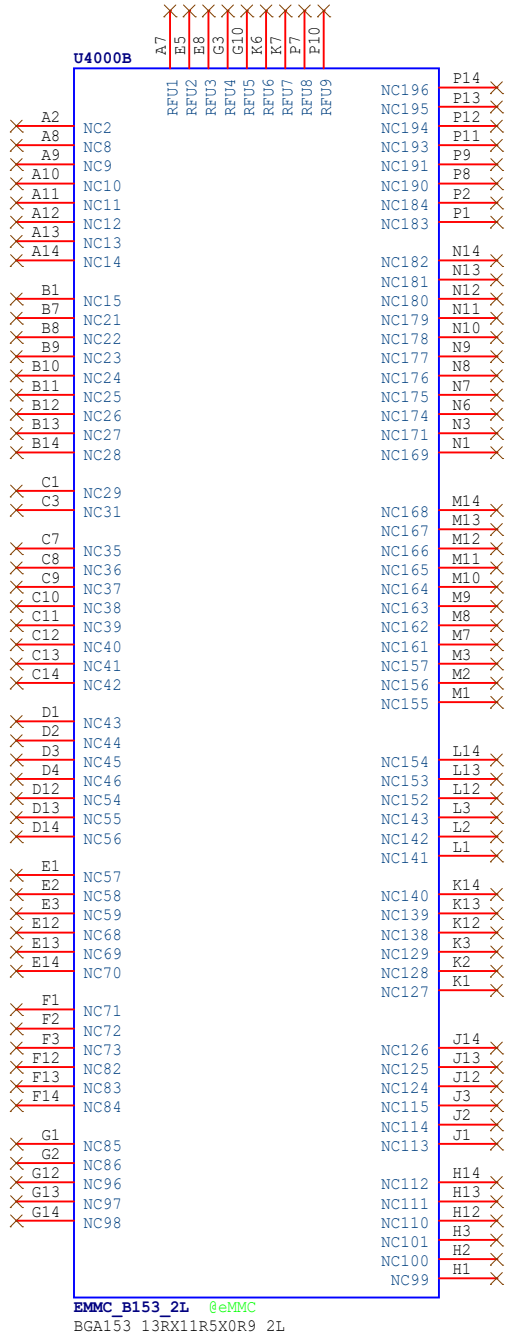




Note:

No need to double layout with Nand Flash, 0R resistor can be omitted





Note:

If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	40.Flash-eMMC Flash				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	33 of 72

Nand Flash

eMMC_D0/FLASH_D0
eMMC_D1/FLASH_D1
eMMC_D2/FLASH_D2
eMMC_D3/FLASH_D3
eMMC_D4/FLASH_D4
eMMC_D5/FLASH_D5
eMMC_D6/FLASH_D6
eMMC_D7/FLASH_D7

eMMC_CMD/FLASH_WRn

eMMC_CLKOUT/FLASH_DQS

eMMC_DATA_STROBE/FLASH_CLE

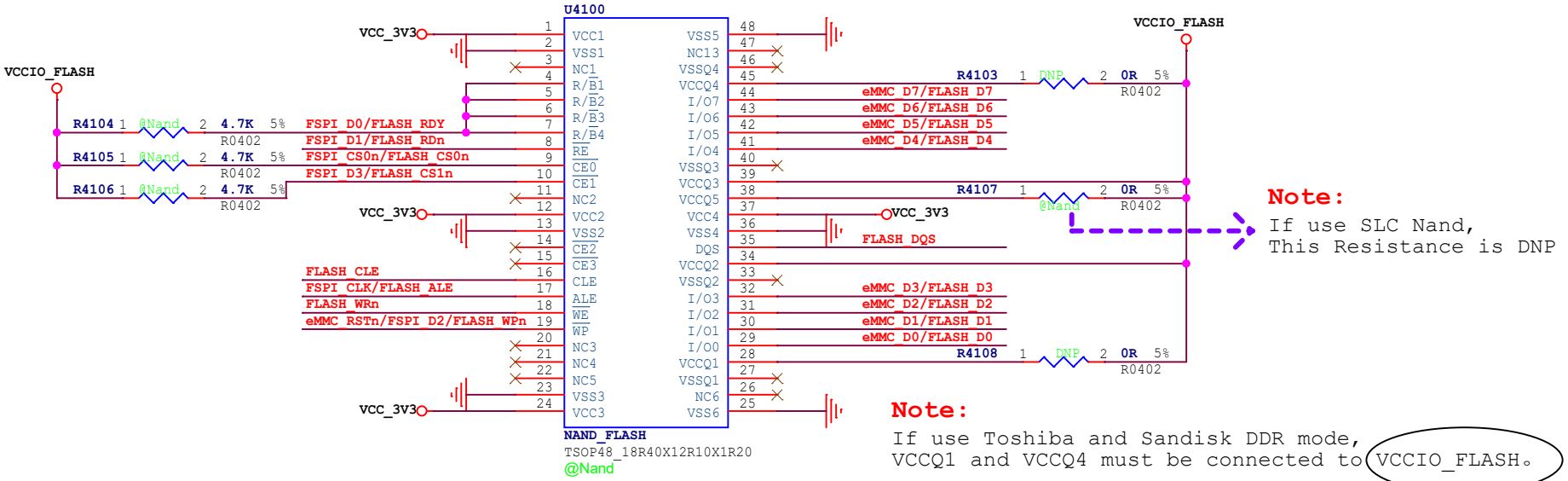
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_CLK/FLASH_ALE
FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
FSPI_CS0n/FLASH_CS0n
FSPI_D3/FLASH_CS1n

eMMC_DATA_STROBE/FLASH_CLE — R4100 1 @Nand 2 0R 5% — FLASH_CLE
R0402
Place at branch point and eMMC_DATA_STROBE Signal

eMMC_CLKOUT/FLASH_DQS — R4101 1 @Nand 2 0R 5% — FLASH_DQS
R0402
Place at branch point and eMMC_CLKOUT Signal

eMMC_CMD/FLASH_WRn — R4102 1 @Nand 2 0R 5% — FLASH_WRn
R0402
Place at branch point and eMMC_CMD Signal

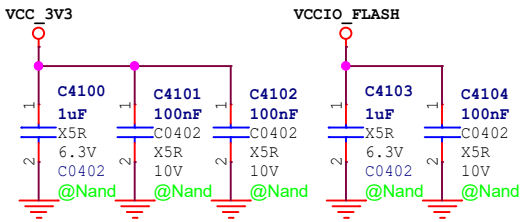
Note:
No need to double layout with eMMC, 0R resistor can be omitted



Note:
If use SLC Nand,
This Resistance is DNP

Note:
If use Toshiba and Sandisk DDR mode,
VCCQ1 and VCCQ4 must be connected to VCCIO_FLASH。

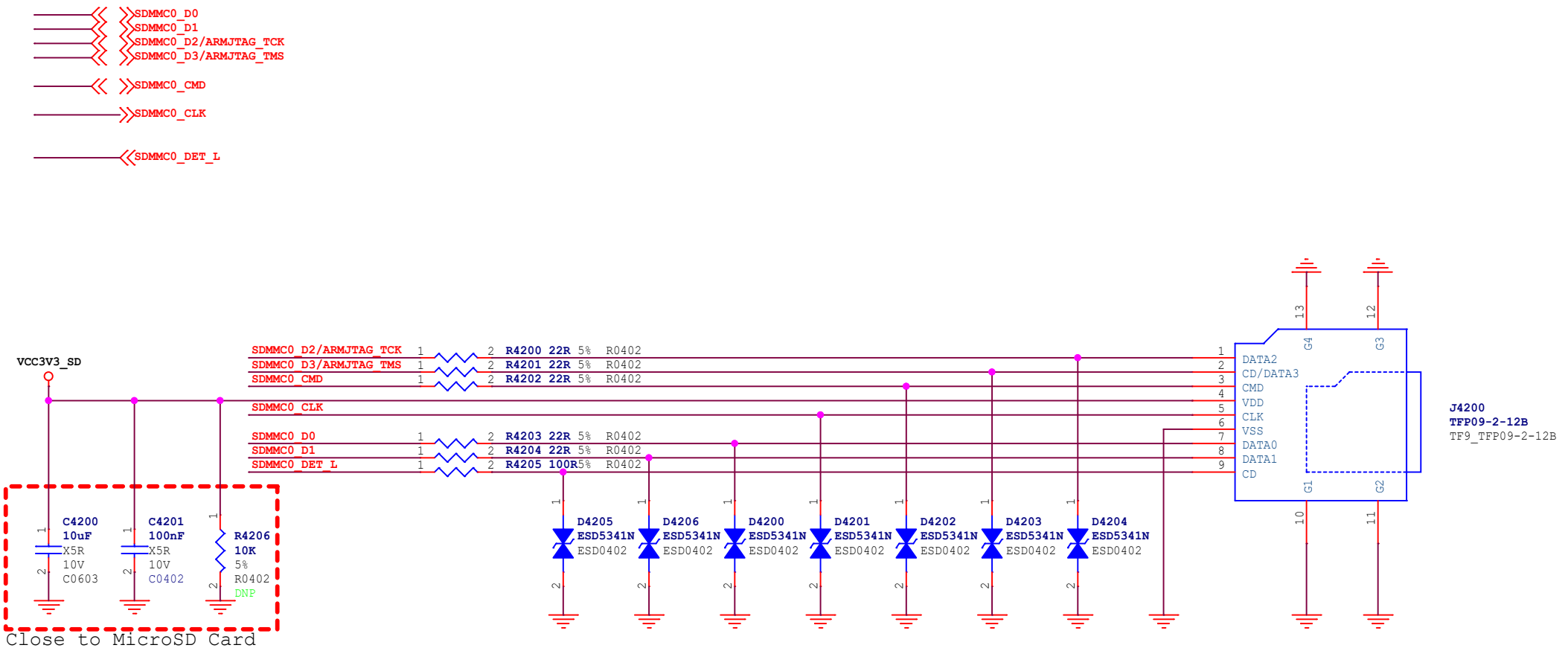
V1.1



Note:
If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	41.Flash-Nand Flash(Option)				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	34 of 72

MicroSD Card



MicroSD Card

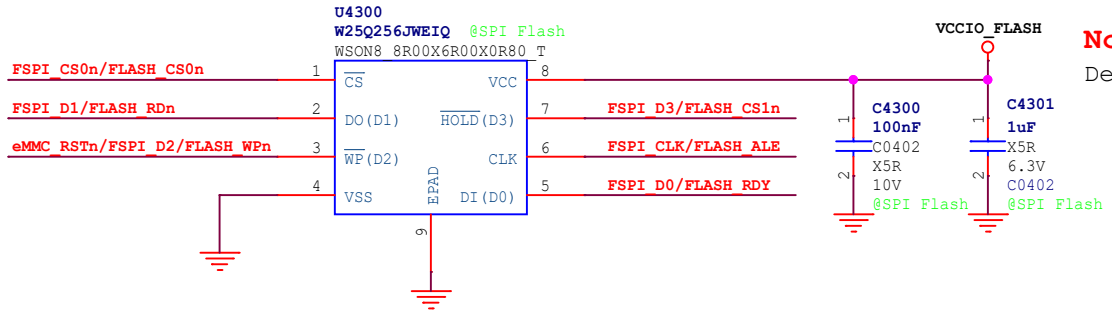
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	42.Flash-MicroSD Card				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	35 of 72

SPI Flash

FSPI_CLK/FLASH_ALE

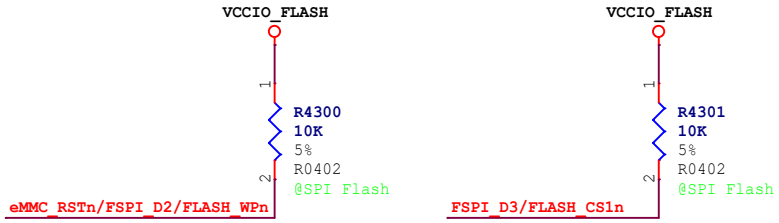
FSPI_D0/FLASH_RDY
FSPI_D1/FLASH_RDn
eMMC_RSTn/FSPI_D2/FLASH_WPn
FSPI_D3/FLASH_CS1n

FSPI_CS0n/FLASH_CS0n



Note:
Default: 1.8V

Support:
1bit SPI NOR or SPI NAND
4bit SPI NOR or SPI NAND

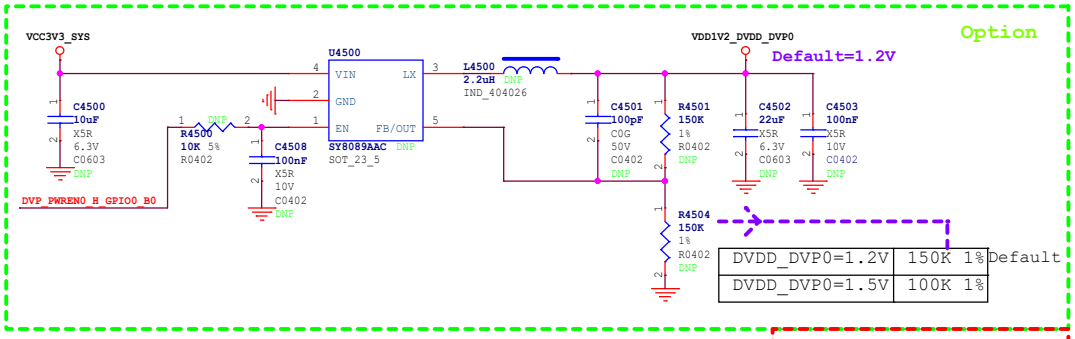


Note:
If Flash is compatible, please notice
when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted,@SPI Flash is not mounted
when Nand is used, the option is that @Nand is mounted, @eMMC is not mounted,@SPI Flash is not mounted
when SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted,@Nand is not mounted

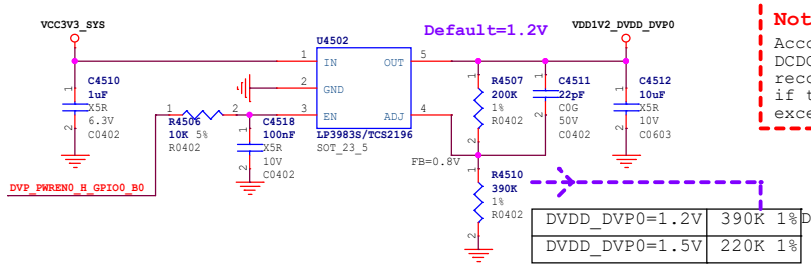
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	43.Flash-SPI FLASH(Option)				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	36 of 72

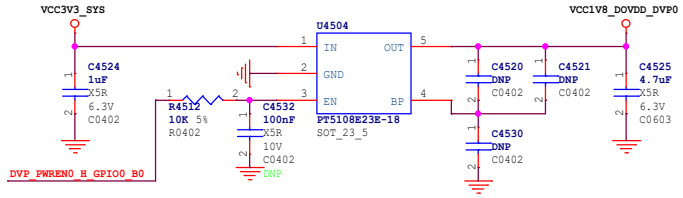
DVP_PWREN0_H_GPIO0_B0
HDMIRX_PWREN_H_GPIO0_D6

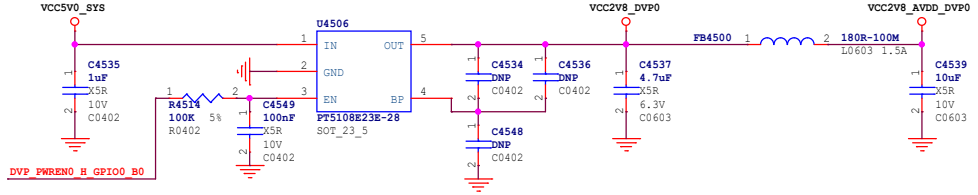
Camera0 Power supply



Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA



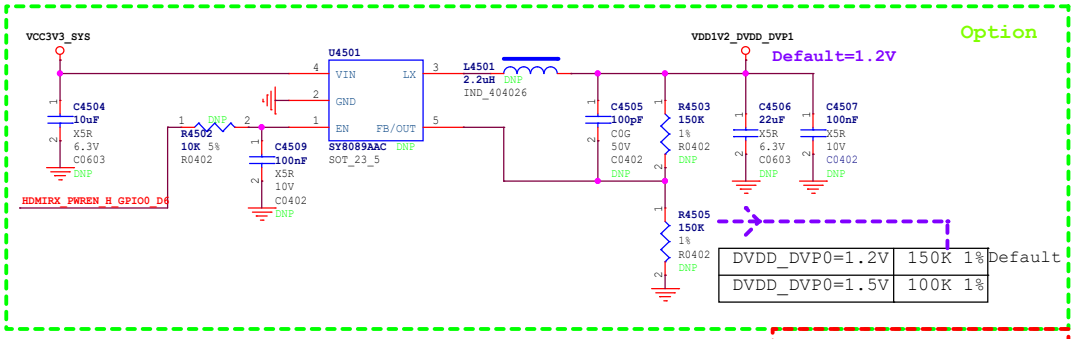




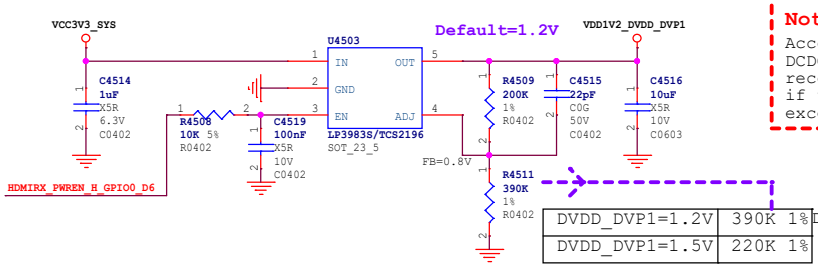
Note:
Adjust the power on sequence according to the camera model
eg:GC8034
Power on Sequence
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST

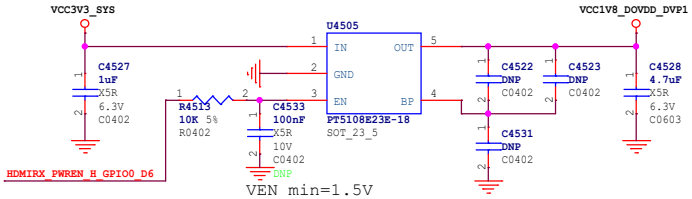
Camera1 Power supply

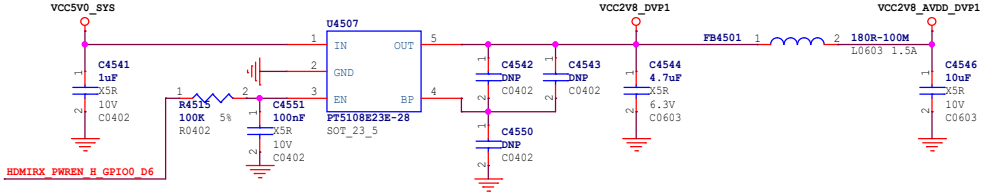
Note:
When the binocular camera is used,
If separate control is required,
separate power supply is recommended



Note:
According to camera model, DCDC power supply is recommended if the DVDD current exceeds 100mA

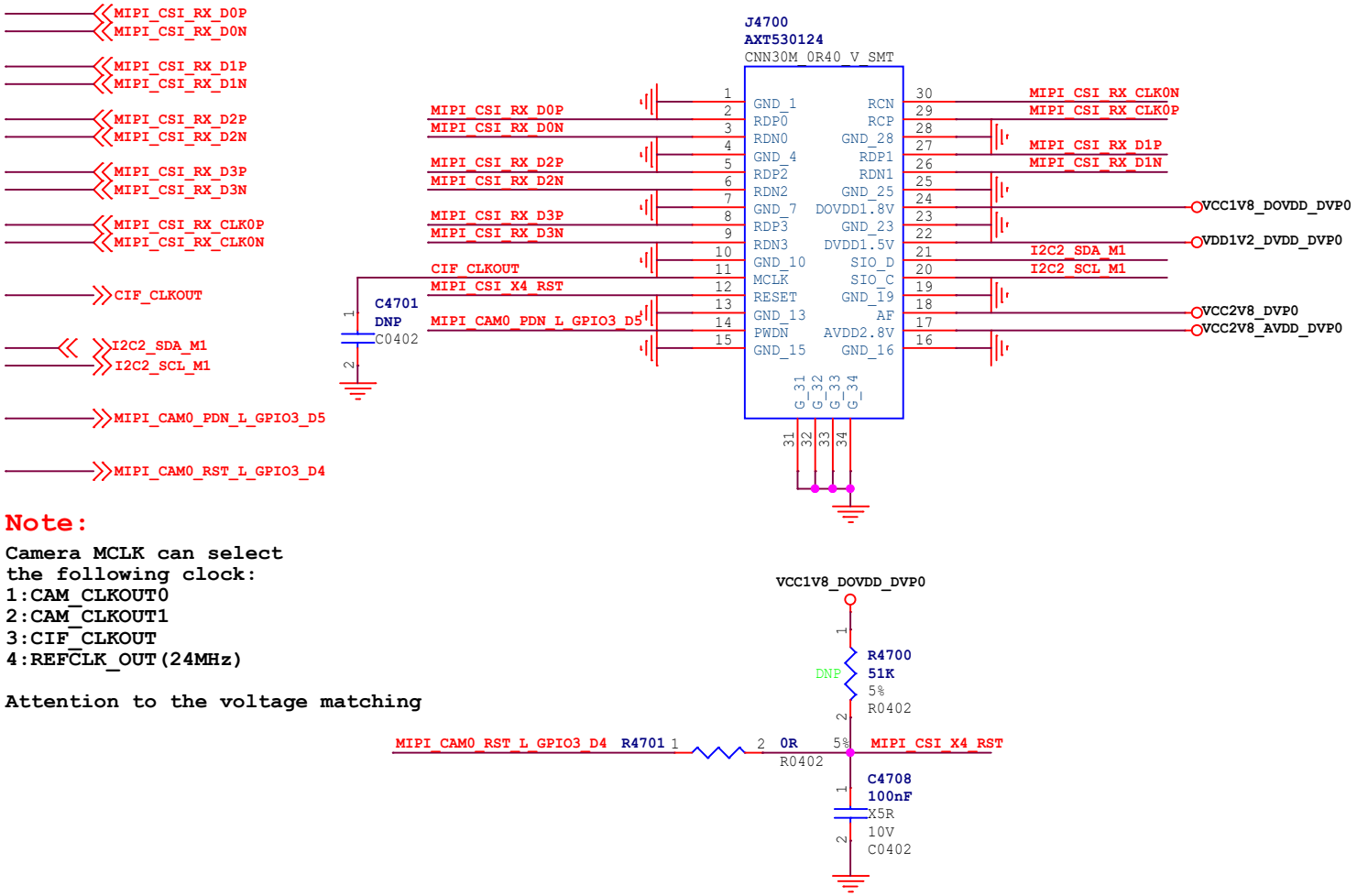






Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	45.VI-Camera_Power				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	37 of 72

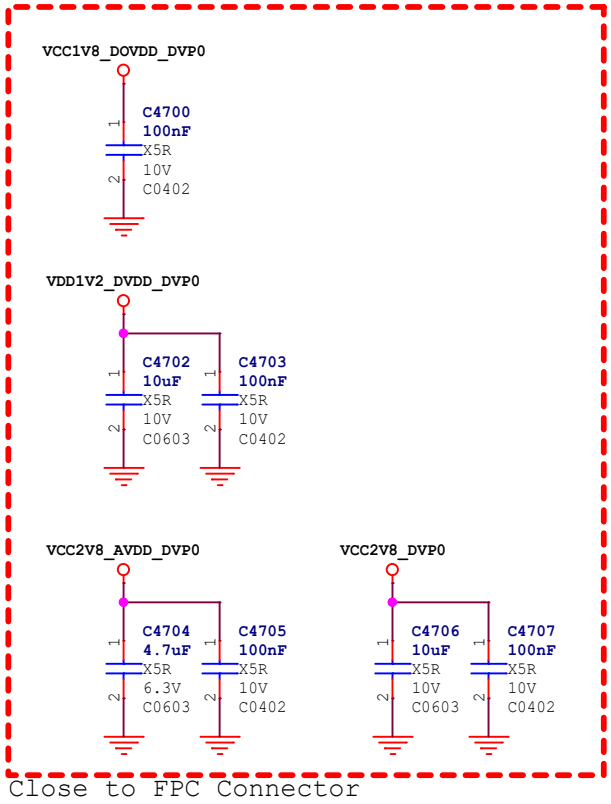
Camera0:MIPI_CSI_RX 4Lanes



Note:

Camera MCLK can select
the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

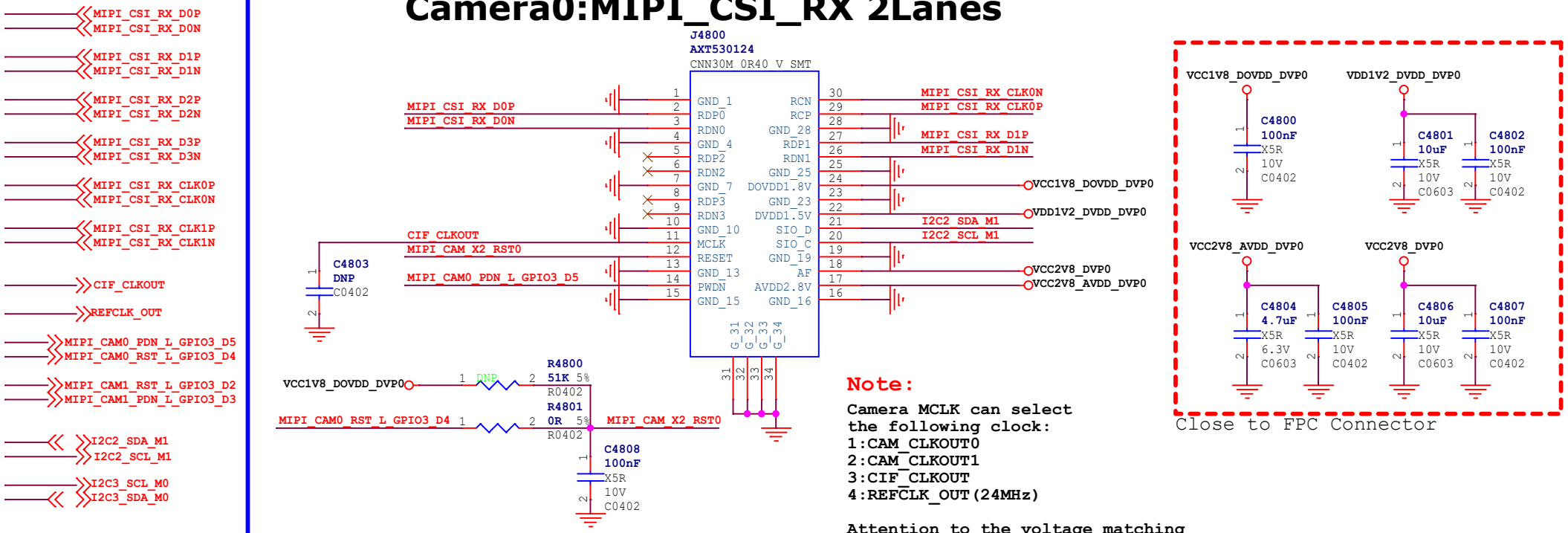


Close to FPC Connector

Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	47.VI-Camera_MIPI_CSI_1x 4Lanes				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	38 of 72

Camera0:MIPI_CSI_RX 2Lanes

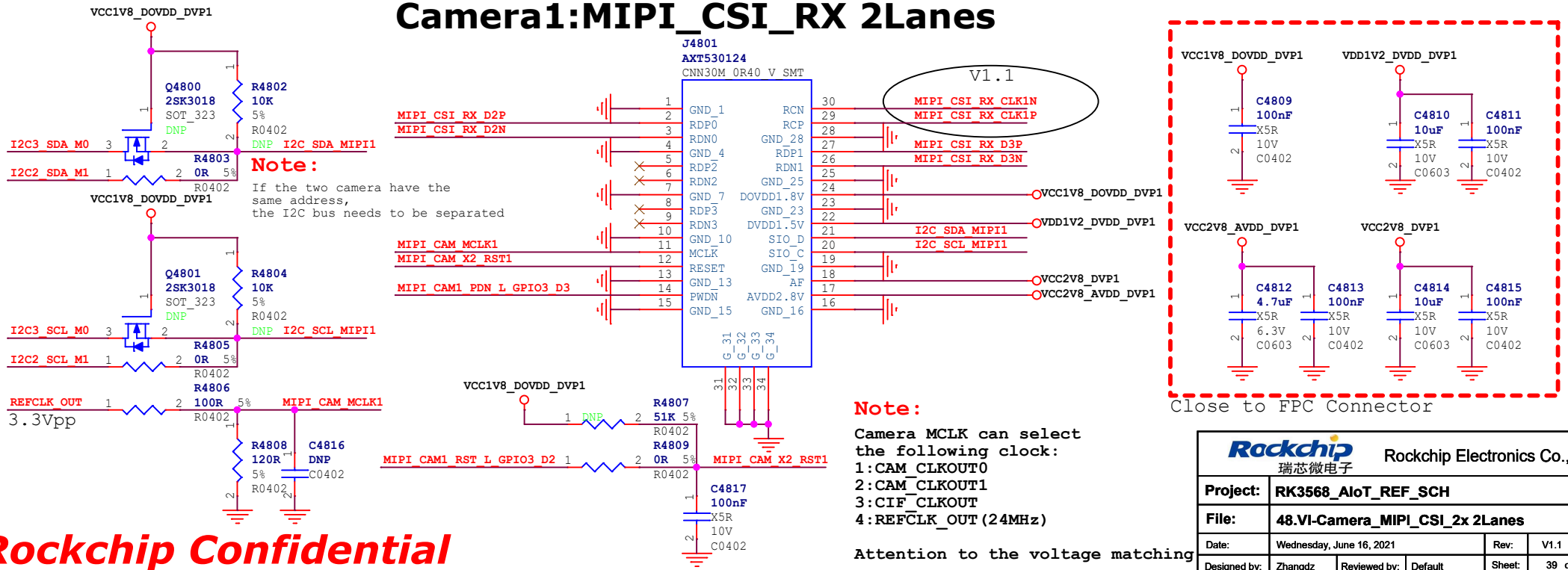


Note:

Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

Camera1:MIPI_CSI_RX 2Lanes



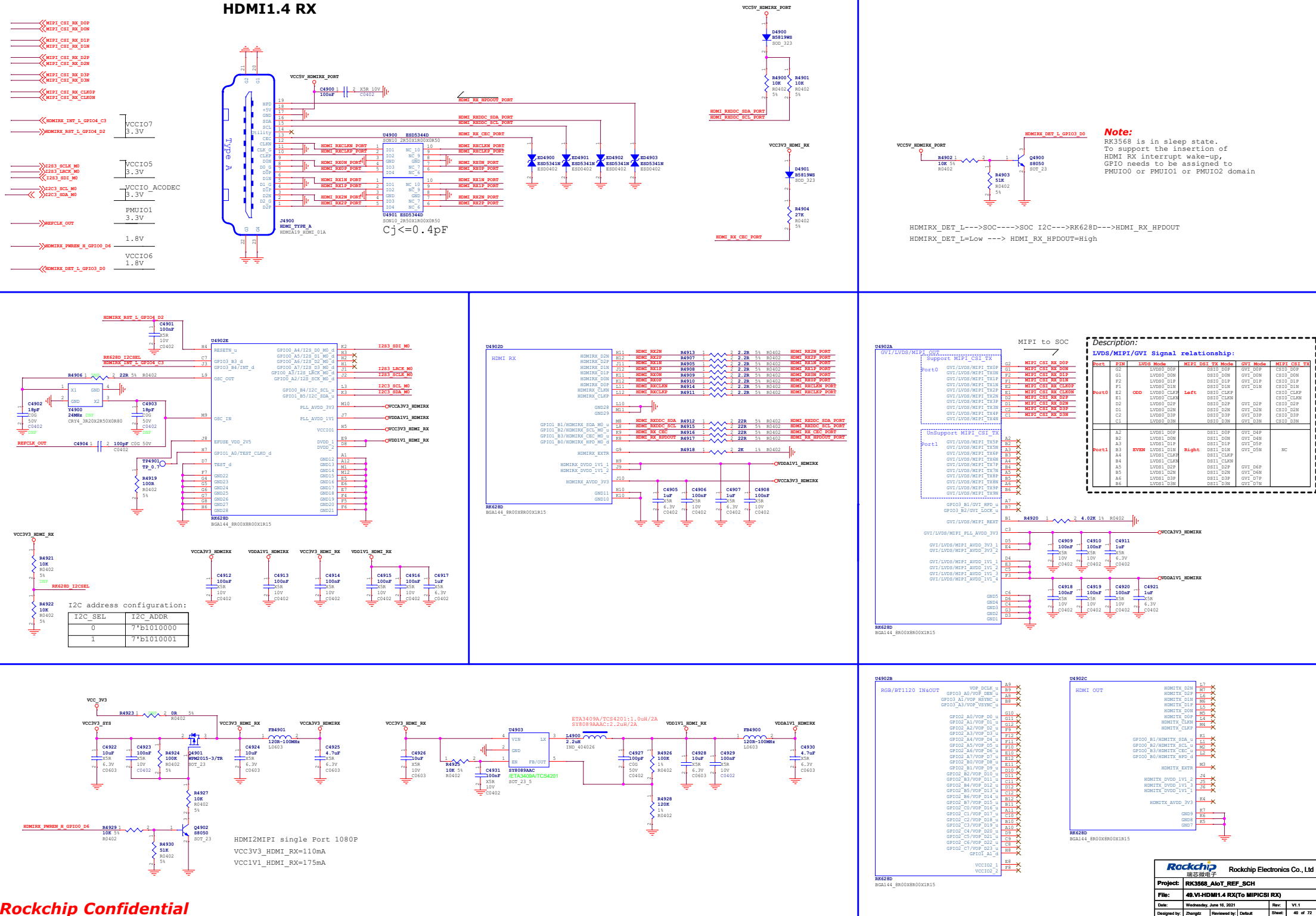
Note:

Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT(24MHz)

Attention to the voltage matching

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	48.VI-Camera_MIPI_CSI_2x 2Lanes				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	39 of 72

HDMI1.4 RX


MIPI_CSI_RX_D0P
MIPI_CSI_RX_D0N
MIPI_CSI_RX_D1P
MIPI_CSI_RX_D1N
MIPI_CSI_RX_D2P
MIPI_CSI_RX_D2N
MIPI_CSI_RX_D3P
MIPI_CSI_RX_D3N
MIPI_CSI_RX_CLK0P
MIPI_CSI_RX_CLK0N
HDMIRX_INT_L_GPIO4_C3
HDMIRX_RST_L_GPIO4_D2
VCCIO7 3.3V
I2S3_SCLK_M0
I2S3_LRCK_M0
I2S3_SDI_M0
VCCIO5 3.3V
I2C3_SCL_M0
I2C3_SDA_M0
VCCIO_ACODEC 3.3V
REFCLK_OUT
PMUIO1 3.3V
HDMIRX_PWREN_H_GPIO0_D6
1.8V
HDMIRX_DET_L_GPIO3_D0
VCCIO6 1.8V
Type A
J4900
HDMI_TYPE_A
HDMIA19_HDMI_01A
VCC5V_HDMIRX_PORT
C4900 100nF
HDMI_RX_HPDOUT_PORT
HDMI RXDDC_SDA_PORT
HDMI RXDDC_SCL_PORT
HDMI_RX_CEC_PORT
HDMI_RXCLKN_PORT
HDMI_RXCLKP_PORT
HDMI_RX0N_PORT
HDMI_RX0P_PORT
HDMI_RX1N_PORT
HDMI_RX1P_PORT
HDMI_RX2N_PORT
HDMI_RX2P_PORT
U4900 ESD5344D
U4901 ESD5344D
ED4900 ESD5341N
ED4901 ESD5341N
ED4902 ESD5341N
ED4903 ESD5341N
Cj<=0.4pF
VCC3V3_HDMI_RX
D4900 BS819WS
D4901 BS819WS
R4900 10K
R4901 10K
R4904 27K
HDMIRX_DET_L_GPIO3_D0
R4902 10K
R4903 51K
Q4900 S8050
Note:
RK3568 is in sleep state.
To support the insertion of HDMI RX interrupt wake-up, GPIO needs to be assigned to PMUIO0 or PMUIO1 or PMUIO2 domain
HDMIRX_DET_L---->SOC---->SOC I2C--->RK628D--->HDMI_RX_HPDOUT
HDMIRX_DET_L=Low ---> HDMI_RX_HPDOUT=High
HDMIRX_RST_L_GPIO4_D2
C4901 100nF
RK628D_I2CSEL
HDMIRX_INT_L_GPIO4_C3
U4902E
RK628D
BGA144_8R00X8R00X1R15
R4906 22R
Y4900 24MHz
C4902 18pF
C4903 18pF
REFCLK_OUT
C4904 100pF
TP4901 TP_0.7
R4919 100R
I2S3_SDI_M0
I2S3_LRCK_M0
I2S3_SCLK_M0
I2C3_SCL_M0
I2C3_SDA_M0
VCCA3V3_HDMIRX
VDDA1V1_HDMIRX
VCC3V3_HDMI_RX
VDD1V1_HDMI_RX
U4902D
HDMI RX
R4913
R4907
R4905
R4908
R4909
R4910
R4914
R4911
R4912
R4915
R4916
R4917
R4918
C4905 1uF
C4906 100nF
C4907 1uF
C4908 100nF
R4921 10K
R4922 10K
RK628D_I2CSEL
I2C address configuration:
I2C_SEL | I2C_ADDR
0 | 7'b1010000
1 | 7'b1010001
C4912 100nF
C4913 100nF
C4914 100nF
C4915 100nF
C4916 100nF
C4917 1uF
U4902A
GVI/LVDS/MIPI_OUT
MIPI to SOC
Support MIPI_CSI_TX
UnSupport MIPI_CSI_TX
Port0
Port1
R4920 4.02K
C4909 100nF
C4910 100nF
C4911 1uF
C4918 100nF
C4919 100nF
C4920 100nF
C4921 1uF
Description:
LVDS/MIPI/GVI Signal relationship:
Port | PIN | LVDS Mode | MIPI DSI TX Mode | GVI Mode | MIPI_CSI_TX
Port0 | G2 | LVDS0_D0P | DSI0_D0P | GVI_D0P | CSI0_D0P
Port0 | G1 | LVDS0_D0N | DSI0_D0N | GVI_D0N | CSI0_D0N
Port0 | F2 | LVDS0_D1P | DSI0_D1P | GVI_D1P | CSI0_D1P
Port0 | F1 | LVDS0_D1N | DSI0_D1N | GVI_D1N | CSI0_D1N
Port0 | E2 | ODD | Left | DSI0_CLKP | - | CSI0_CLKP
Port0 | E1 | LVDS0_CLKN | DSI0_CLKN | CSI0_CLKN
Port0 | D2 | LVDS0_D2P | DSI0_D2P | GVI_D2P | CSI0_D2P
Port0 | D1 | LVDS0_D2N | DSI0_D2N | GVI_D2N | CSI0_D2N
Port0 | C2 | LVDS0_D3P | DSI0_D3P | GVI_D3P | CSI0_D3P
Port0 | C1 | LVDS0_D3N | DSI0_D3N | GVI_D3N | CSI0_D3N
Port1 | A2 | LVDS1_D0P | DSI1_D0P | GVI_D4P
Port1 | B2 | LVDS1_D0N | DSI1_D0N | GVI_D4N
Port1 | A3 | LVDS1_D1P | DSI1_D1P | GVI_D5P
Port1 | B3 | EVEN | LVDS1_D1N | Right | DSI1_D1N | GVI_D5N | NC
Port1 | A4 | LVDS1_CLKP | DSI1_CLKP
Port1 | B4 | LVDS1_CLKN | DSI1_CLKN
Port1 | A5 | LVDS1_D2P | DSI1_D2P | GVI_D6P
Port1 | B5 | LVDS1_D2N | DSI1_D2N | GVI_D6N
Port1 | A6 | LVDS1_D3P | DSI1_D3P | GVI_D7P
Port1 | B6 | LVDS1_D3N | DSI1_D3N | GVI_D7N
RK628D
BGA144_8R00X8R00X1R15
VCC_3V3
VCC3V3_SYS
VCC3V3_HDMI_RX
VCCA3V3_HDMIRX
R4923 0R
C4922 10uF
C4923 100nF
R4924 100K
U4901 HDM2015-3/TR
C4924 10uF
FB4901 120R-100MHz
C4925 4.7uF
R4927 10K
HDMIRX_PWREN_H_GPIO0_D6
R4929 10K
Q4902 S8050
R4930 51K
HDMI2MIPI single Port 1080P
VCC3V3_HDMI_RX=110mA
VCC1V1_HDMI_RX=175mA
U4903
ETA3409A/TCS4201:1.0uH/2A
SY8089AAC:2.2uH/2A
SY8089AAC /ETA3409A/TCS4201
SOT_23_5
L4900 2.2uH
IND_404026
C4926 10uF
R4925 10K
C4931 100nF
C4927 100pF
R4926 100K
R4928 120K
C4928 10uF
C4929 100nF
FB4900 120R-100MHz
C4930 4.7uF
U4902B
RGB/BT1120 IN&OUT
U4902C
HDMI OUT
RK628D
BGA144_8R00X8R00X1R15
Rockchip Confidential
Rockchip Electronics Co., Ltd
瑞芯微电子
Project: RK3568_AIoT_REF_SCH
File: 49.V1-HDMI1.4 RX(To MIPICSI RX)
Date: Wednesday, June 16, 2021
Rev: V1.1
Designed by: Zhangtz
Reviewed by: Default
Sheet: 40 of 72

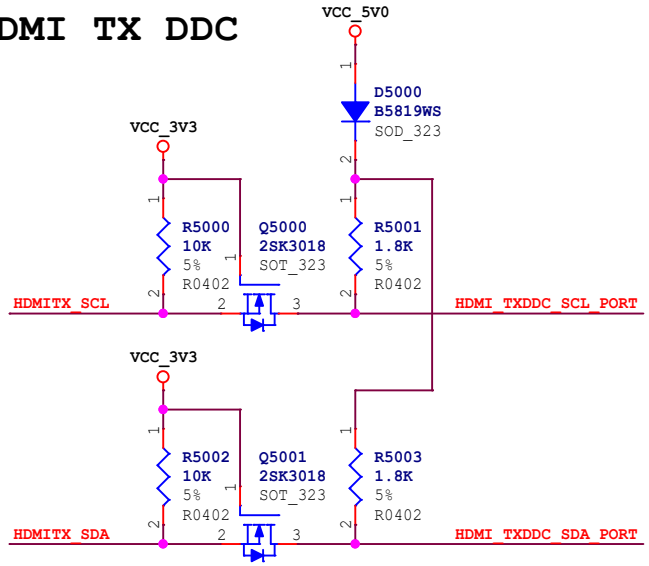
HDMI2.0 TX

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT

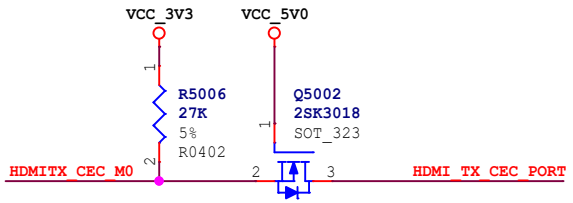
HDMITX_SCL
HDMITX_SDA

HDMITX_CEC_M0
HDMI_TX_HPDIN

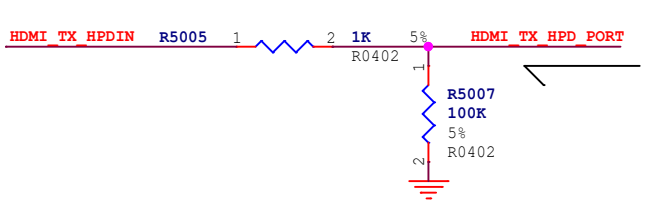
HDMI TX DDC

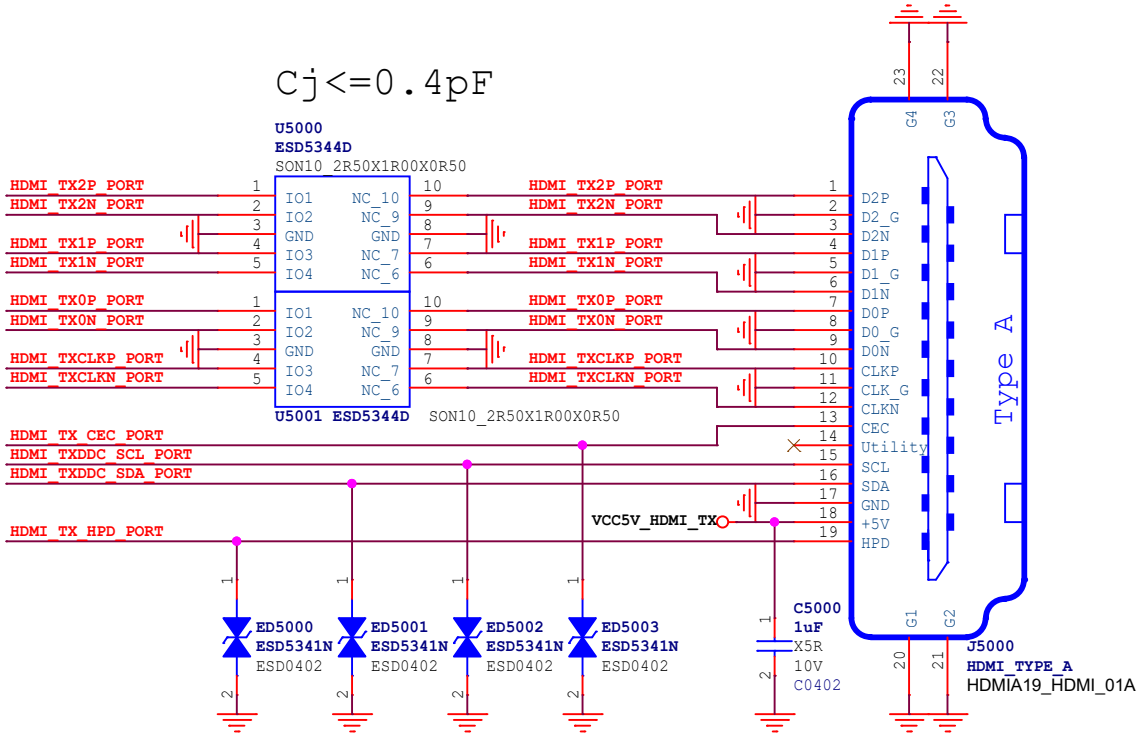


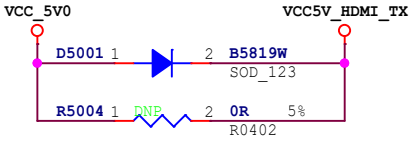
HDMI TX CEC



HDMI TX HPD







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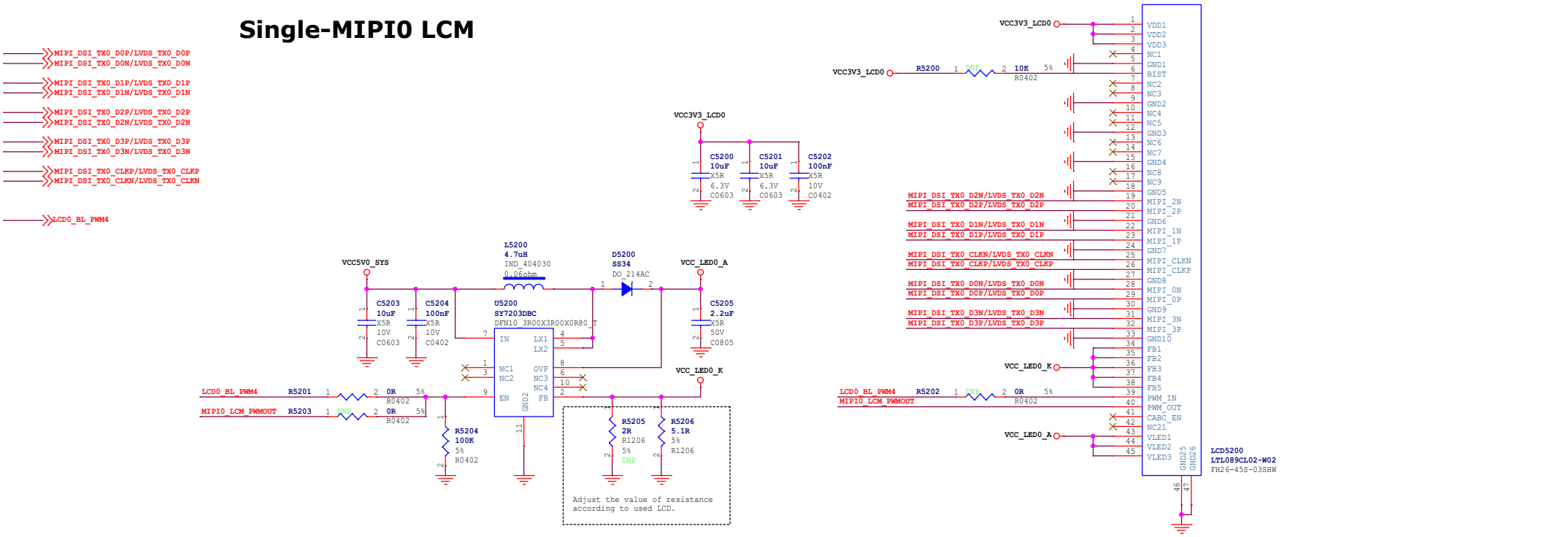
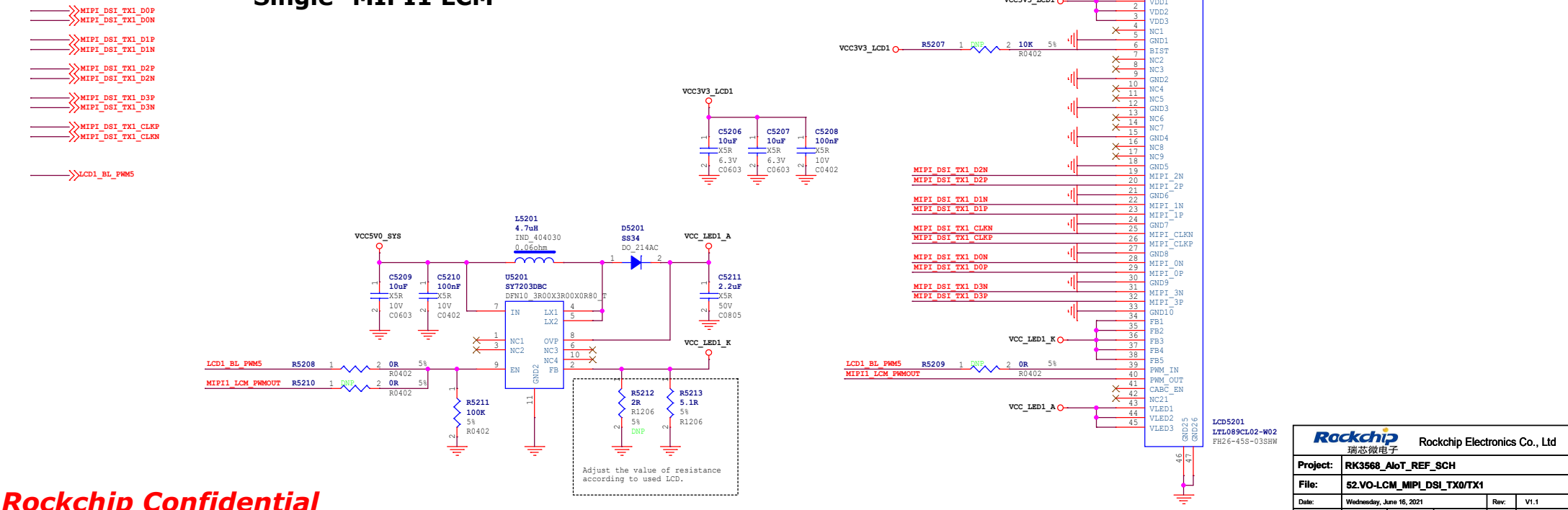
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	50.VO-HDMI2.0 TX				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	41 of 72

Single-MIPI0 LCM



Single- MIPI1 LCM



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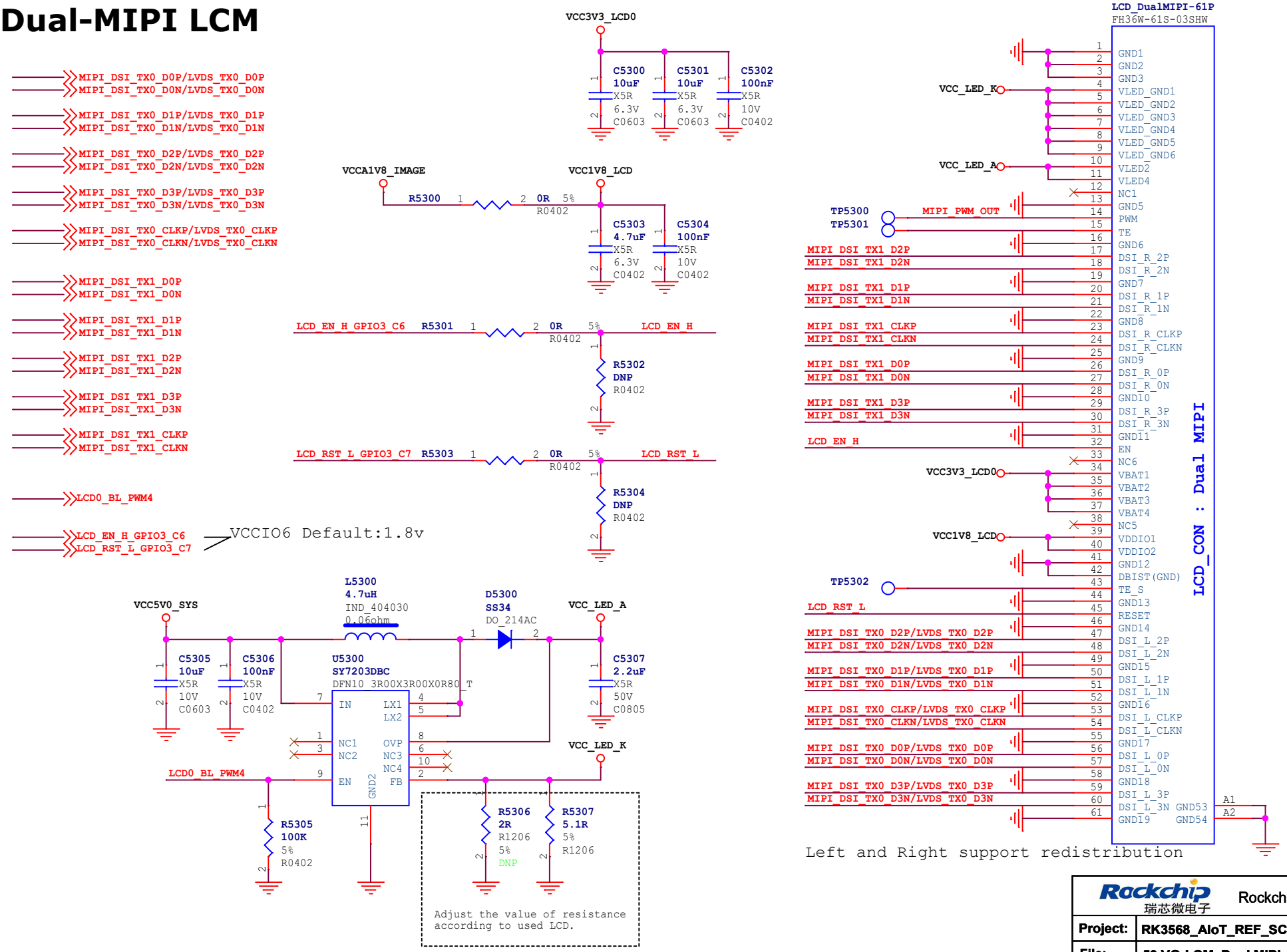
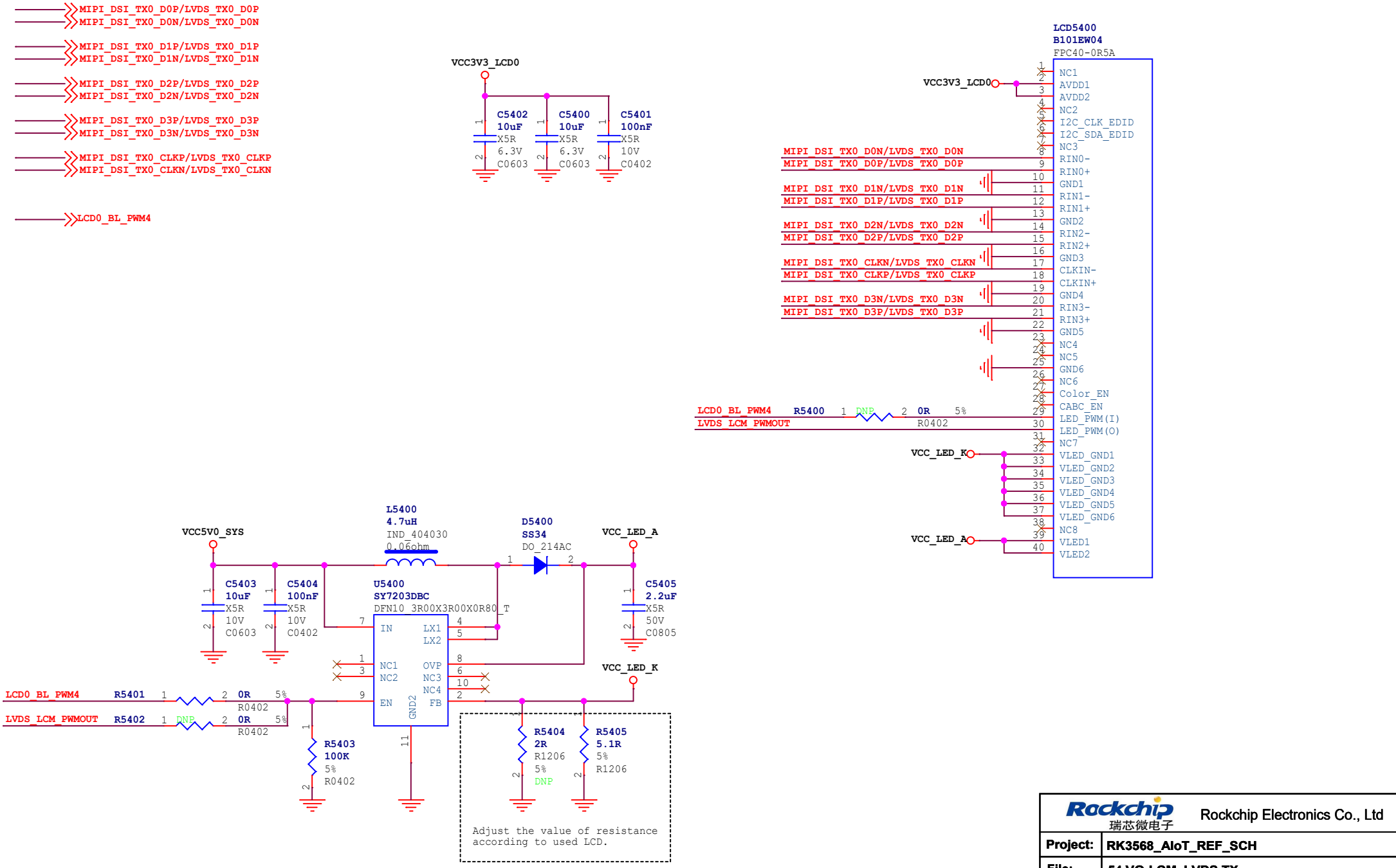
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	52.VO-LCM_MIPI_DSI_TX0/TX1				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	42 of 72

Dual-MIPI LCM



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	53.VO-LCM_Dual MIPI_DSI TX				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	43 of 72

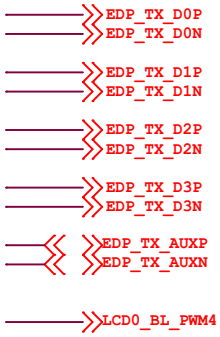
Single-LVDS LCM

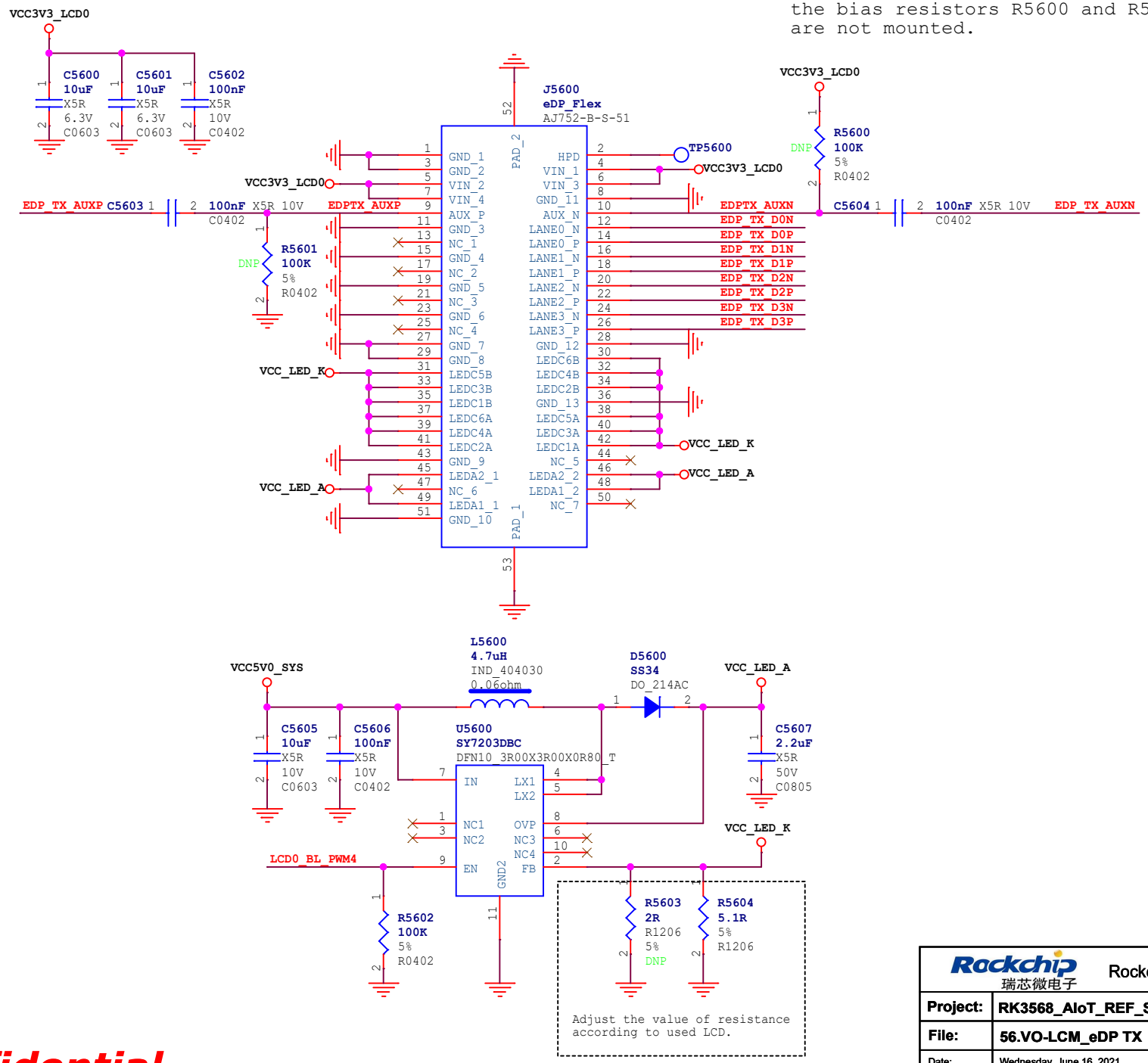


Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	54.VO-LCM_LVDS TX				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	44 of 72

Single-eDP LCM





Note:

For EDP displays with edp1.2a or above, the bias resistors R5600 and R5601 of aux are not mounted.

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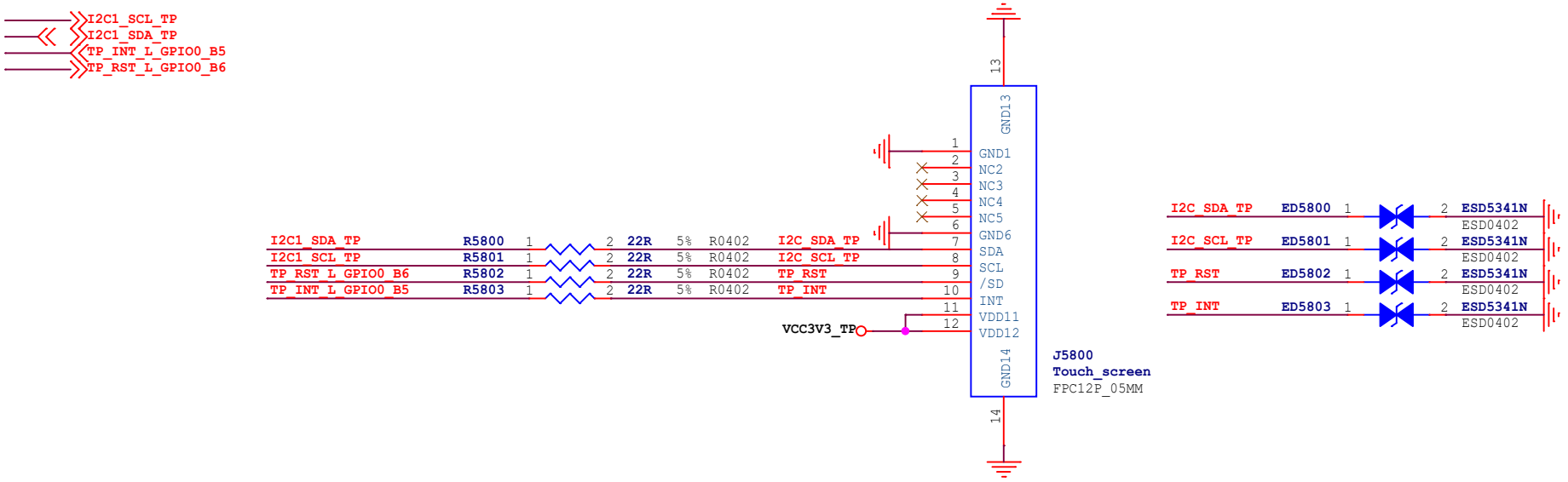
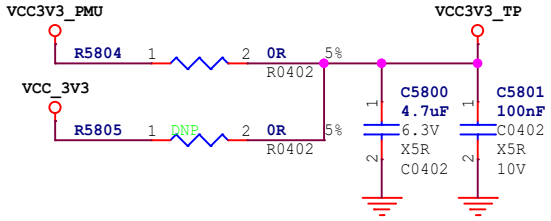
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	56.VO-LCM_eDP TX				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	45 of 72

Touch Panel connector





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Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	58.TP Connector_COF				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	46 of 72

VGA OUT

Default:RTD2166

CH7517,IT6516:Can also support

EDP_TX_D0P
EDP_TX_D0N
EDP_TX_D1P
EDP_TX_D1N
EDP_TX_AUXP
EDP_TX_AUXN
VGA_HPDIN_GPIO0_C0
VGA_PWREN_H_GPIO0_D5
I2C5_SCL_M0
I2C5_SDA_M0

PMUIO2
3.3V
1.8V

Power Sequence:
5v-->3.3v-->1.2v

BLM18BB220SN1D

550mW

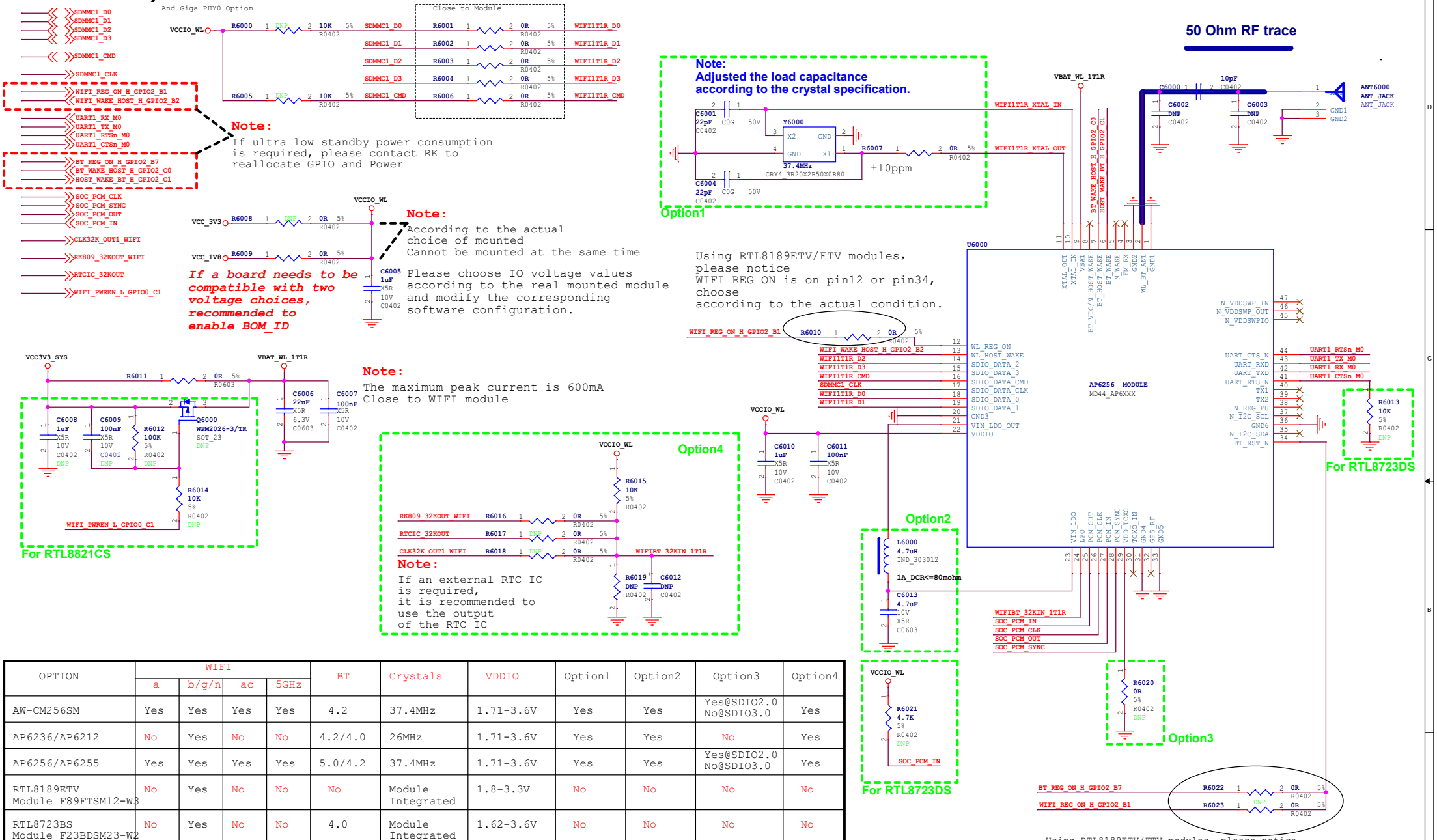
BAT54S

RTD2166
QFN32_4R00X4R00X0R90_T

J5900
VGA_DB15
DSUB15B

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	59.VO-VGA Output(eDP To VGA)				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	47 of 72

SDIO WIFI/BT MODULE



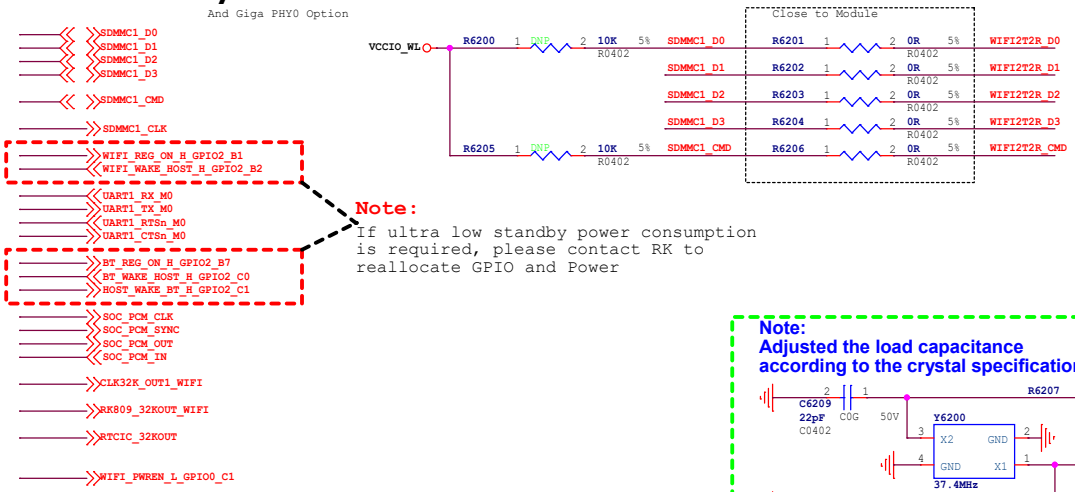
OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3	Option4
	a	b/g/n	ac	5GHz							
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.6V	Yes	Yes	No	Yes
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.71-3.6V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes
RTL8189ETV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No
RTL8723BS Module F23BDSM23-W2	No	Yes	No	No	4.0	Module Integrated	1.62-3.6V	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.6V	No	No	No	No
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	60.WIFI/BT-SDMMC1_1T1R + UART
Date:	Wednesday, June 16, 2021
Rev:	V1.1
Designed by:	Zhangdz
Reviewed by:	Default
Sheet:	48 of 72

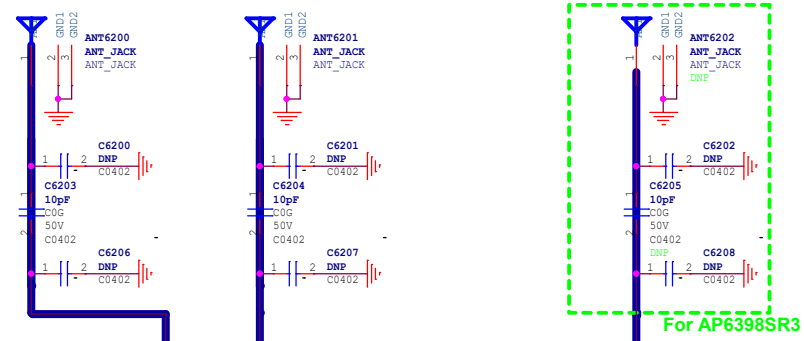
SDIO WIFI/BT MODULE-2T2R

And Giga PHY0 Option

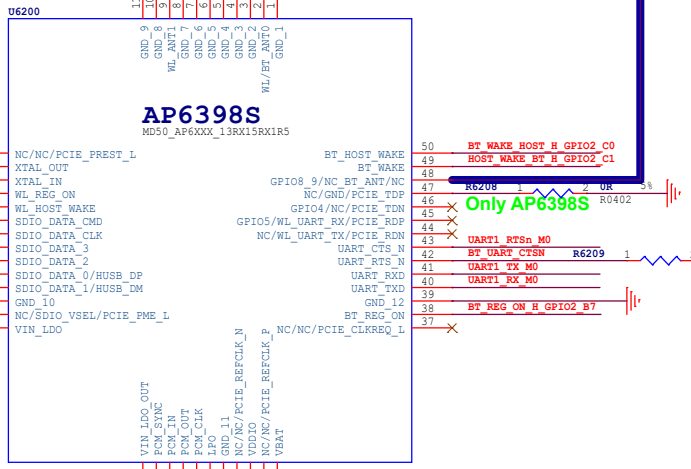


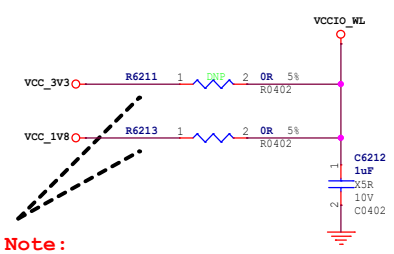
Note:

If ultra low standby power consumption is required, please contact RK to reallocate GPIO and Power



50 Ohm RF trace



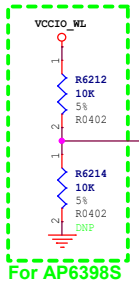


Note:

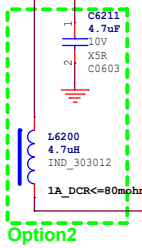
According to the actual choice of mounted
Cannot be mounted at the same time

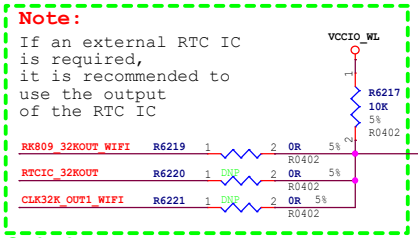
Please choose IO voltage values according to the real mounted module and modify the corresponding software configuration.

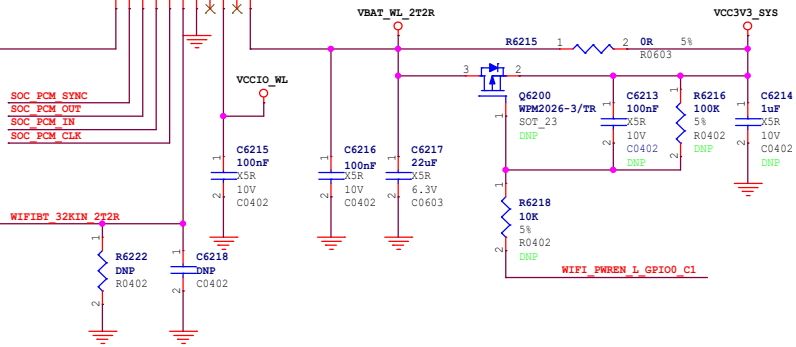
If a board needs to be compatible with two voltage choices, recommended to enable BOM_ID



SDIO voltage select:
0: 3.3V 1:1.8V







OPTION	WIFI				BT	Crystals	VDDIO	Option1	Option2	Option3
	a	b/g/n	ac	5GHz						
AP6398S	Yes	Yes	Yes	Yes	5.0	37.4MHz	1.71-3.6V	Yes	Yes	Yes
AP6356S	Yes	Yes	Yes	Yes	4.1	37.4MHz	1.71-3.6V	Yes	Yes	Yes
RTL8822BS Module	Yes	Yes	Yes	Yes	4.1	Module Integrated	1.71-3.6V	No	No	No

Note:
Yes: option circuit be mounted
No: option circuit not be mounted

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	62.WIFI/BT-SDMMC1_2T2R + UART				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	49 of 72

PCIe WIFI6/BT MODULE-2T2R

WIFI_REG_ON_H_GPIO2_B1
WIFI_WAKE_HOST_H_GPIO2_B2
UART1_RX_M0
UART1_TX_M0
UART1_RTSn_M0
UART1_CTSn_M0
BT_REG_ON_H_GPIO2_B7
BT_WAKE_HOST_H_GPIO2_C0
HOST_WAKE_BT_H_GPIO2_C1
SOC_PCM_CLK
SOC_PCM_SYNC
SOC_PCM_OUT
SOC_PCM_IN
CLK32K_OUT1_WIFI
RK809_32KOUT_WIFI
RTCIC_32KOUT

Note:
If ultra low standby power consumption is required, please contact RK to reallocate GPIO and Power

PCIE20_TXP
PCIE20_TXN
PCIE20_RXP
PCIE20_RXN
PCIE20_REFCLKP
PCIE20_REFCLKN
PCIE20_CLKREQn_M1
PCIE20_WAKEn_M1
PCIE20_PERSTn_M1

Note:
Adjusted the load capacitance according to the crystal specification.

ANT6400 ANT_JACK
ANT6401 ANT_JACK
ANT6402 ANT_JACK
C6400 DNP C0402
C6401 DNP C0402
C6402 DNP C0402
C6403 10pF C0G 50V C0402
C6404 DNP C0402
C6405 DNP C0402
C6406 DNP C0402
R6400 0R 5% R0402
R6401 0R 5% R0402
V1.1

50 Ohm RF trace
For AP6275PR3

U6400
AP6275P/AP6275PR3
MD50_AP6XXX_13RX15RX1R5

C6407 22pF C0G 50V C0402
C6409 22pF C0G 50V C0402
Y6400 37.4MHz CRY4_3R20X2R50X0R80
R6402 0R 5% R0402

PCIE20_PERSTn_1V8
WIFI_REG_ON_H_GPIO2_B1
WIFI_WAKE_HOST_H_GPIO2_B2
SOC_PCM_IN
SOC_PCM_OUT
SOC_PCM_SYNC
SOC_PCM_CLK
PCIE20_WAKEn_1V8

BT_WAKE_HOST_H_GPIO2_C0
HOST_WAKE_BT_H_GPIO2_C1
PCIE_TDP C6408 100nF C0201 X5R 10V PCIE20_RXP
PCIE_TDN C6410 100nF C0201 X5R 10V PCIE20_RXN
PCIE_RDP C6411 100nF C0201 X5R 10V PCIE20_TXP
PCIE_RDN C6412 100nF C0201 X5R 10V PCIE20_TXN
UART1_RTSn_M0
UART1_CTSn_M0
UART1_TX_M0
UART1_RX_M0
BT_REG_ON_H_GPIO2_B7
PCIE20_CLKREQn_1V8

C6413 4.7uF 10V X5R C0603

VCCIO_WL
Q6400 2SK3018 SOT_323
R6403 10K 5% R0402
PCIE20_CLKREQn_M1
PCIE20_CLKREQn_1V8

Q6401 2SK3018 SOT_323
R6405 10K 5% R0402
PCIE20_WAKEn_M1
PCIE20_WAKEn_1V8

PCIE20_PERSTn_M1 R6407 10K 5% R0402 PCIE20_PERSTn_1V8
R6408 12K 5% R0402

L6400 2.2uH IND_303015 1A_DCR<=80mohm
L6401 2.2uH IND_303015 1A_DCR<=80mohm
C6418 4.7uF 10V X5R C0603

VCC3V3_PCIEWL_VBAT
VCC3V3_SYS
R6404 0R 5% R0603
C6414 100nF X5R 10V C0402
C6415 22uF X5R 10V C0805
Max:1.2A

VCCIO_WL
VCC_1V8
R6406 0R 5% R0402
C6416 100nF X5R 10V C0402
C6417 4.7uF 10V X5R C0603
Max:0.3A

PCIE_REFCLKP
PCIE_REFCLKN
C6419 100pF C0201 X5R 25V PCIE20_REFCLKP
C6420 100pF C0201 X5R 25V PCIE20_REFCLKN

R6409 10K 5% R0402
RK809_32KOUT_WIFI R6410 0R 5% R0402
RTCIC_32KOUT R6411 DNP 0R 5% R0402
CLK32K_OUT1_WIFI R6412 DNP 0R 5% R0402
PCIE_WIFIBT_32KIN
R6413 DNP R0402
C6421 DNP C0402

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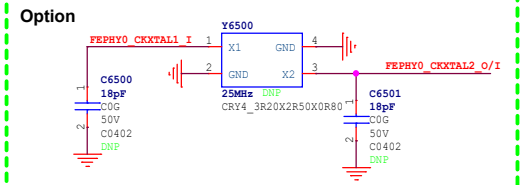
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	64.WIFI6/BT-PCIe_2T2R + UART				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	50 of 72

FE PHY0

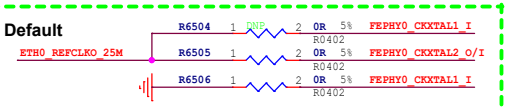
And SDIO WIFI Option

GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXEN
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXDV_CRS
GMAC0_RXER
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
ETH0_REFCLKO_25M
GMAC0_RSTn_GPIO3_B7

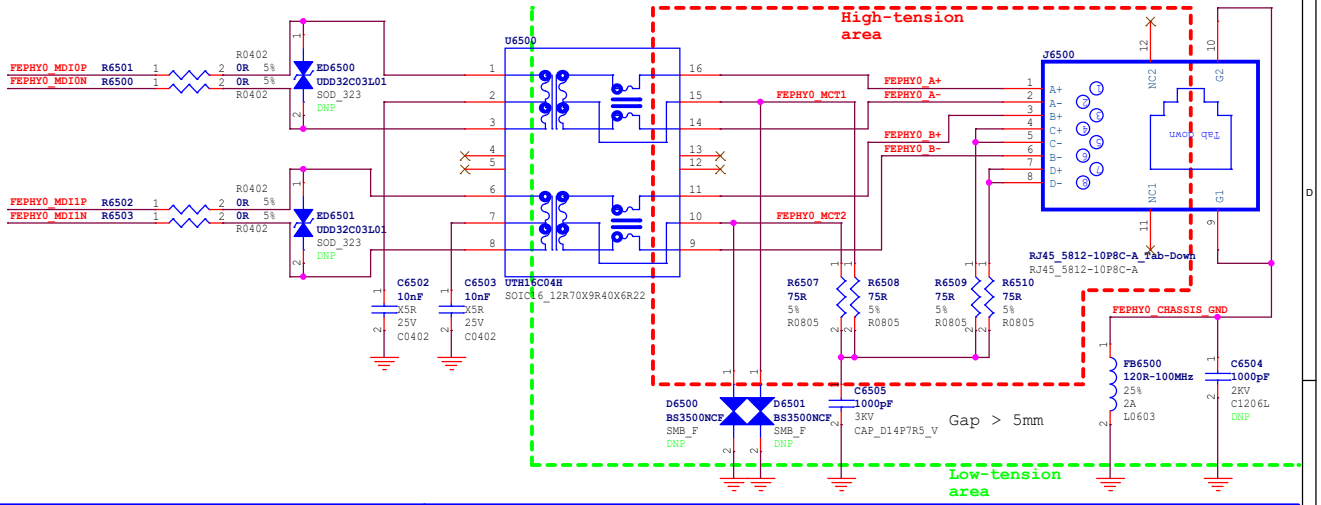
Option



Default

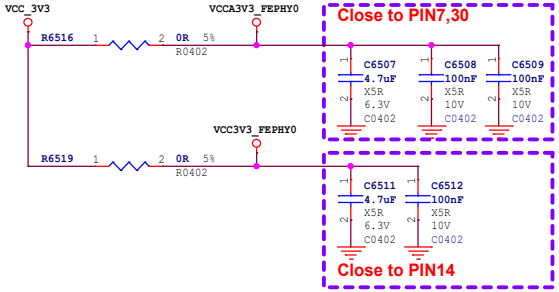


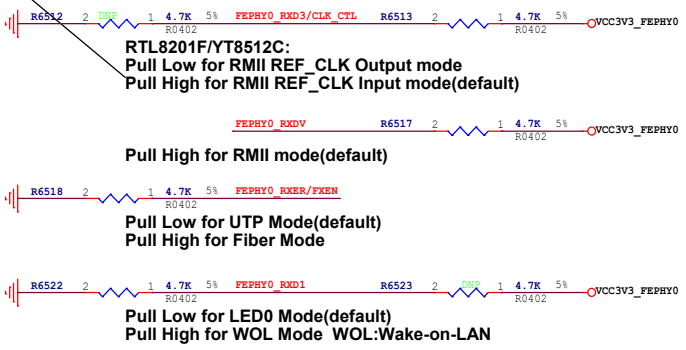
Default: Refclk:MAC output,PHY input



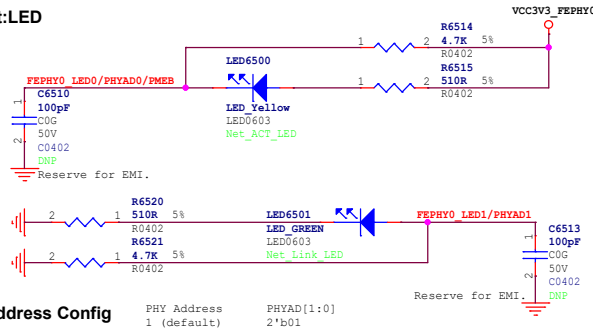
Note:

RTL8201F/YT8512C only support 3.3V IO
VCCIO4 must be changed to 3.3V power supply



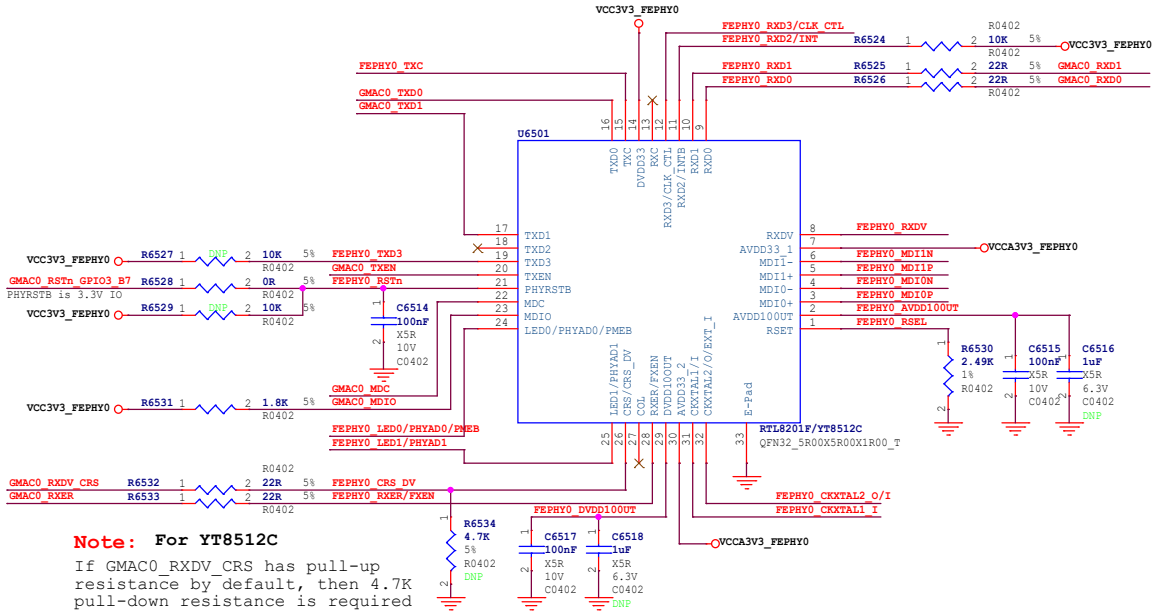


Default:LED



PHY Address Config

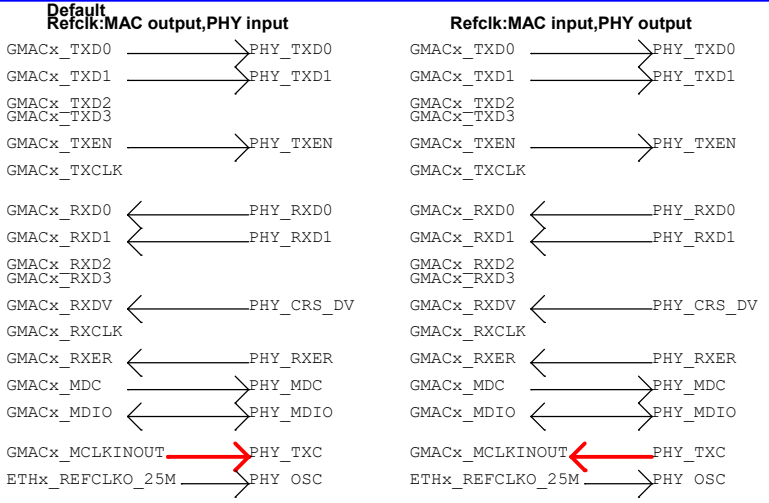
PHY Address	PHYAD[1:0]
1 (default)	2'b01



Note: For YT8512C

If GMAC0_RXDV_CRS has pull-up resistance by default, then 4.7K pull-down resistance is required

Default

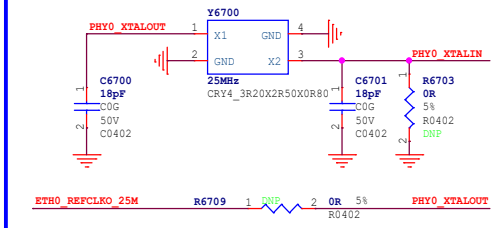


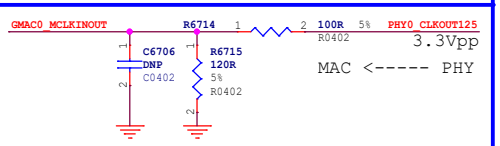
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	65.Ethernet-FEPHY_RMII0				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	51 of 72

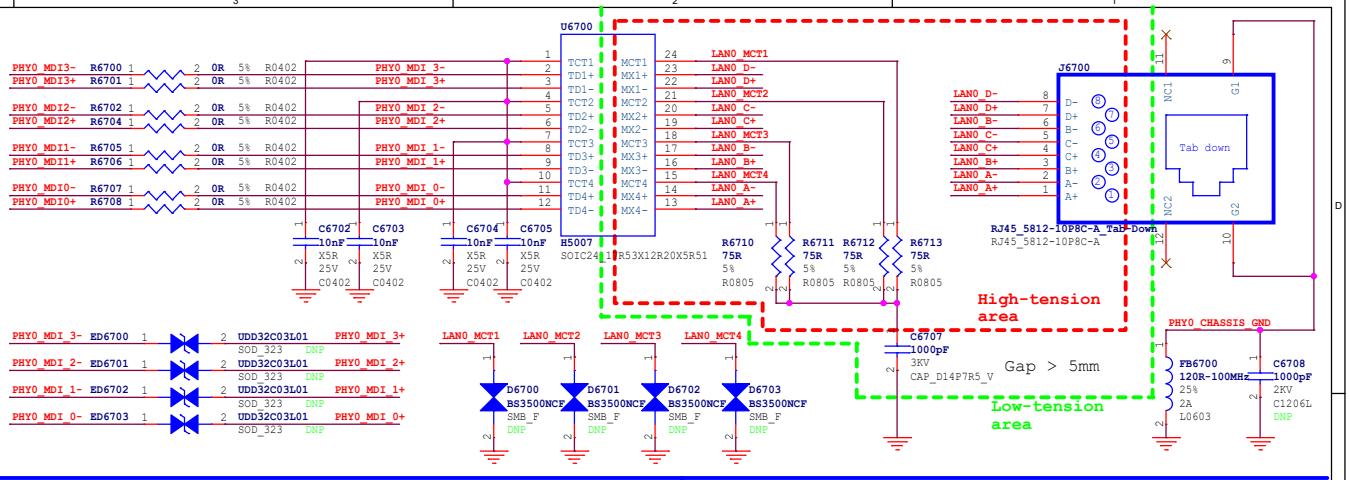
Giga PHY0

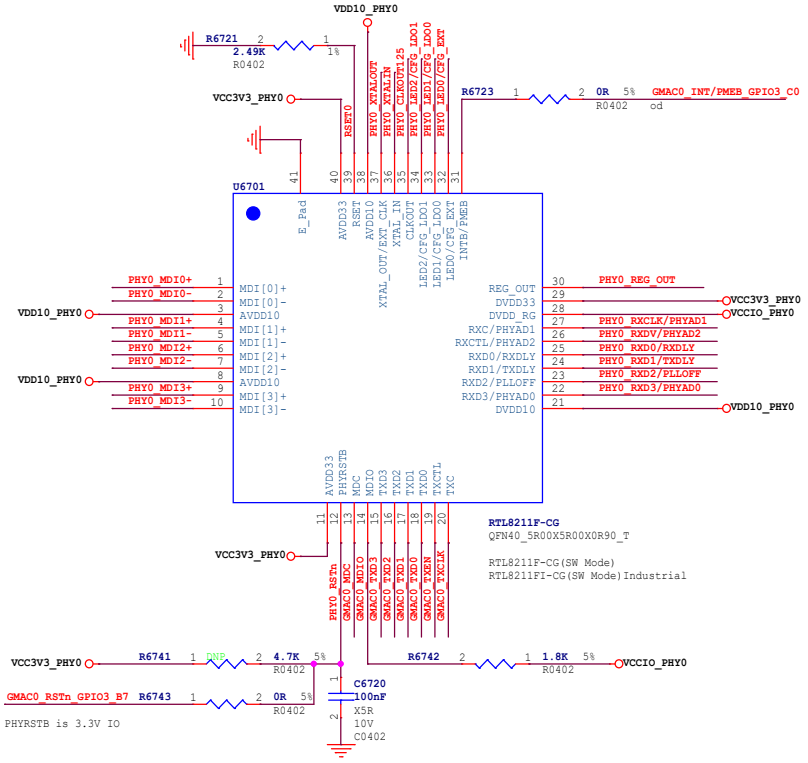
And SDIO WIFI Option

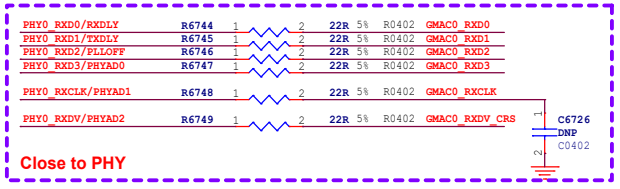
GMAC0_TXD0
GMAC0_TXD1
GMAC0_TXD2
GMAC0_TXD3
GMAC0_TXEN
GMAC0_TXCLK
GMAC0_RXD0
GMAC0_RXD1
GMAC0_RXD2
GMAC0_RXD3
GMAC0_RXDV_CRS
GMAC0_RXCLK
ETH0_REFCLKO_25M
GMAC0_MCLKINOUT
GMAC0_MDC
GMAC0_MDIO
GMAC0_RSTn_GPIO3_B7
GMAC0_INT/PMEB_GPIO3_C0

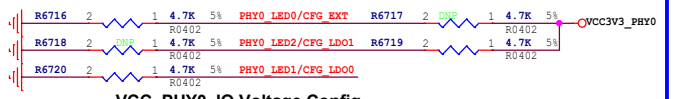




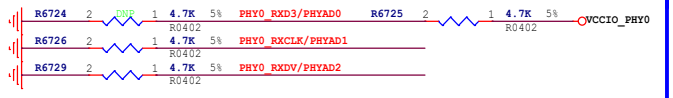








VCC_PHY0_IO Voltage Config



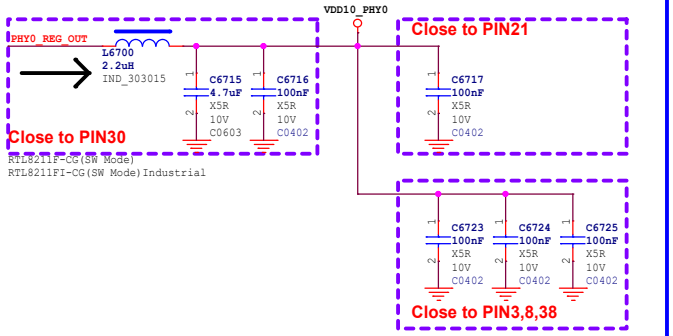
PHY Address Configuration

PHY Address	PHYAD[2:0]
1 (default)	3'b001

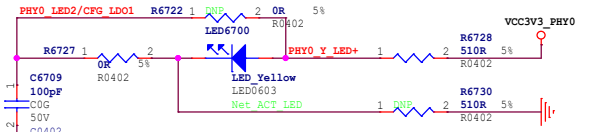
Pull-up for additional 2ns delay to RXC for data latching

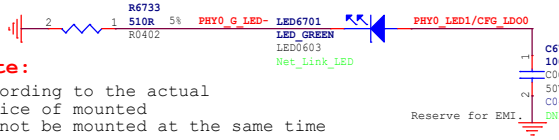
Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDPS mode(Low power mode)



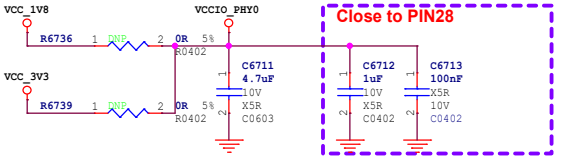
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	

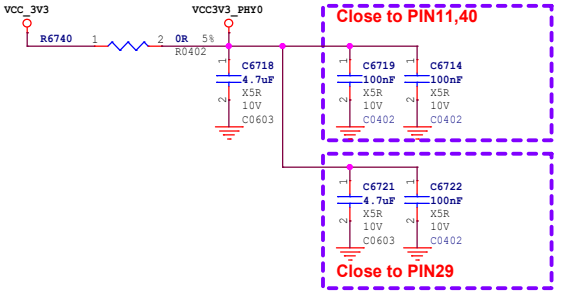




Note:

According to the actual choice of mounted Cannot be mounted at the same time

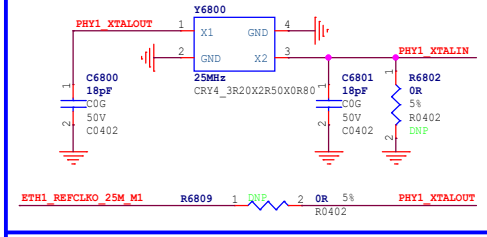


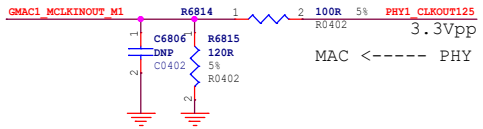


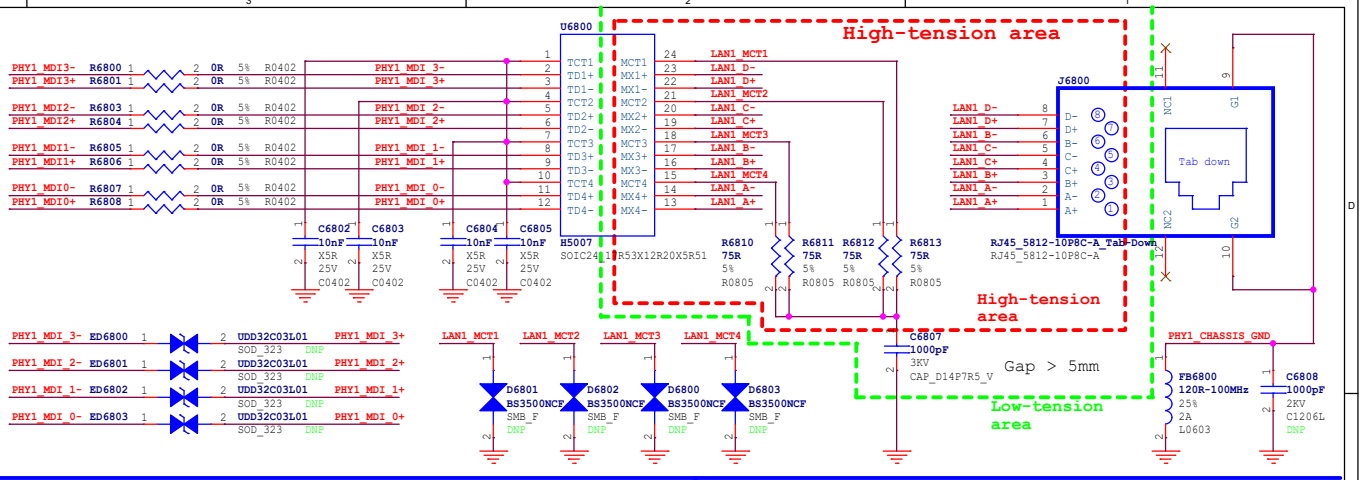
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd			
Project:	RK3568_AIoT_REF_SCH			
File:	67.Ethernet-GEPHY_RGMII0			
Date:	Wednesday, June 16, 2021		Rev:	V1.1
Designed by:	Zhangdz	Reviewed by: Default	Sheet:	52 of 72

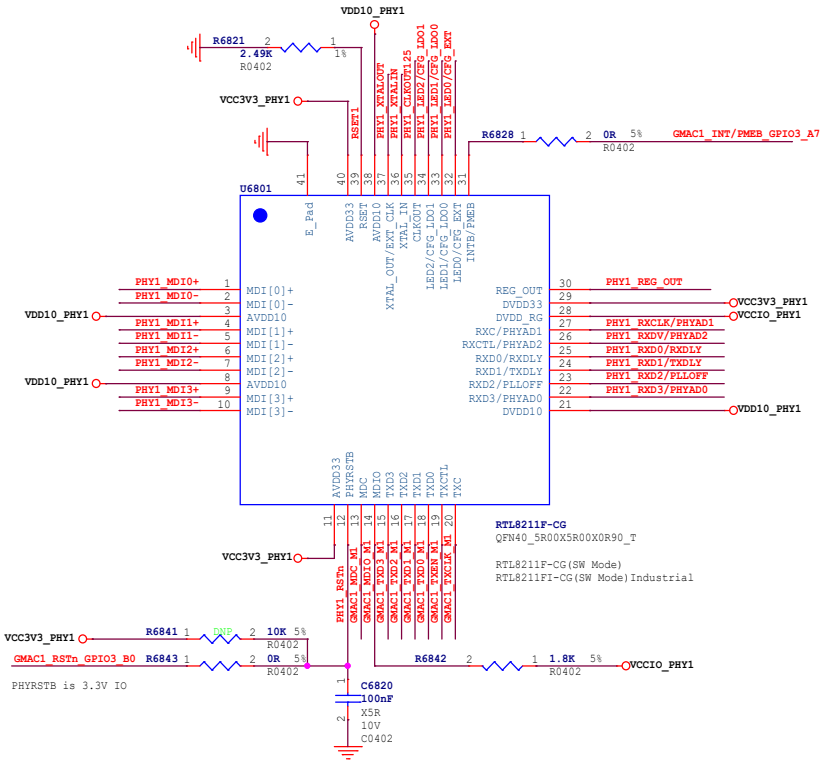
Giga PHY1

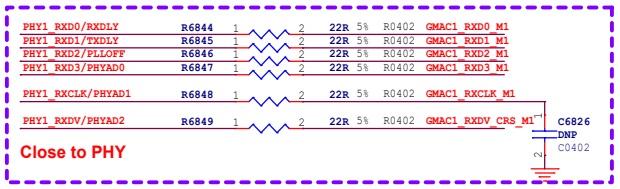
GMAC1_TXD0_M1
GMAC1_TXD1_M1
GMAC1_TXD2_M1
GMAC1_TXD3_M1
GMAC1_TXEN_M1
GMAC1_TXCLK_M1
GMAC1_RXD0_M1
GMAC1_RXD1_M1
GMAC1_RXD2_M1
GMAC1_RXD3_M1
GMAC1_RXDV_CRS_M1
GMAC1_RXCLK_M1
ETH1_REFCLKO_25M_M1
GMAC1_MCLKINOUT_M1
GMAC1_MDC_M1
GMAC1_MDIO_M1
GMAC1_RSTn_GPIO3_B0
GMAC1_INT/PMEB_GPIO3_A7

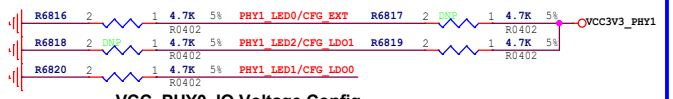


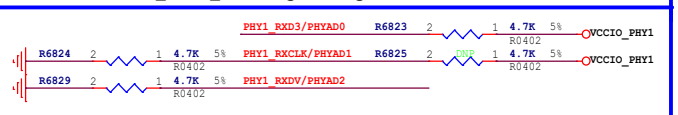


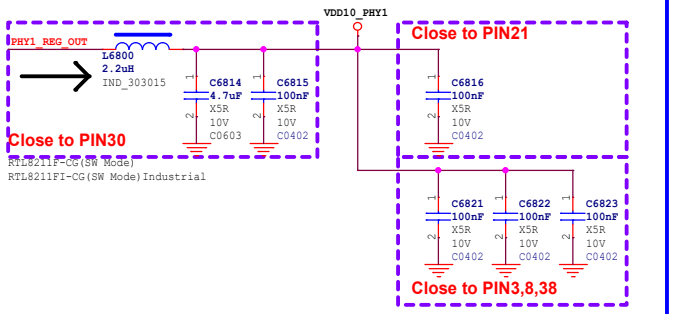




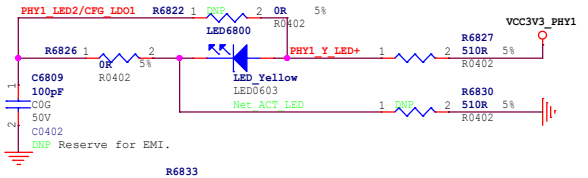


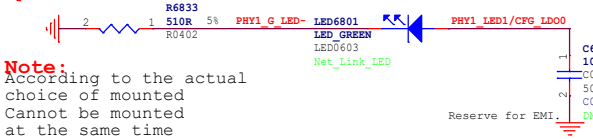




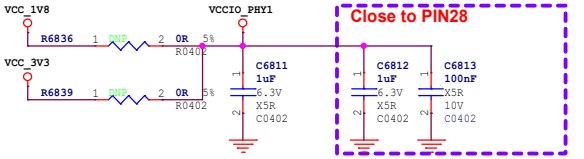


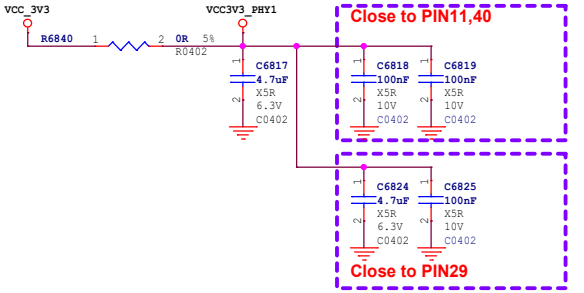
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	





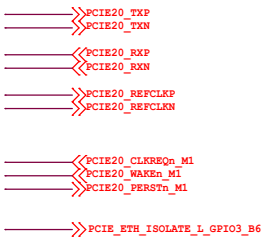
Note:
According to the actual choice of mounted Cannot be mounted at the same time

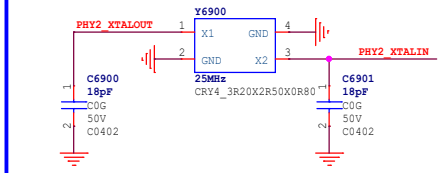


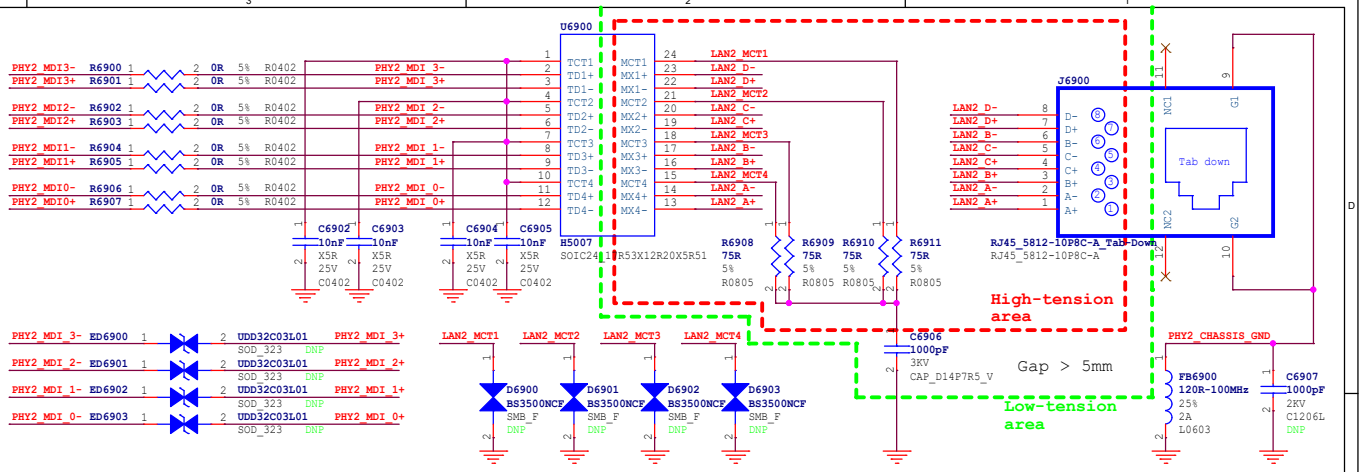


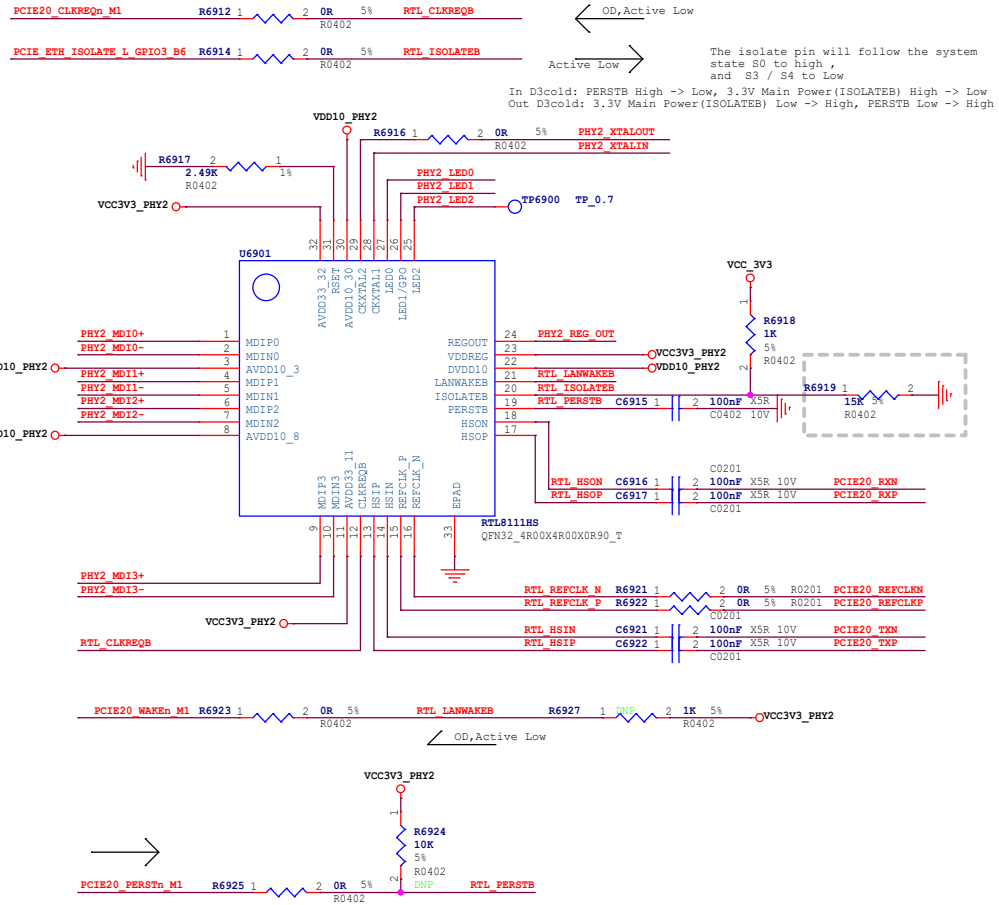
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	68.Ethernet-GEPHY_RGMII1_M1				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	53 of 72

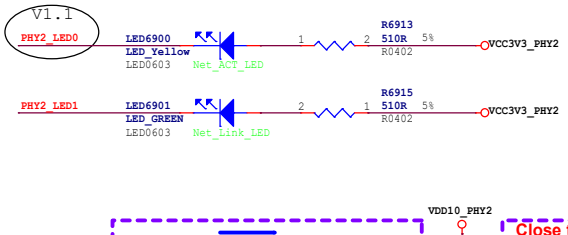
PCIE Ethernet

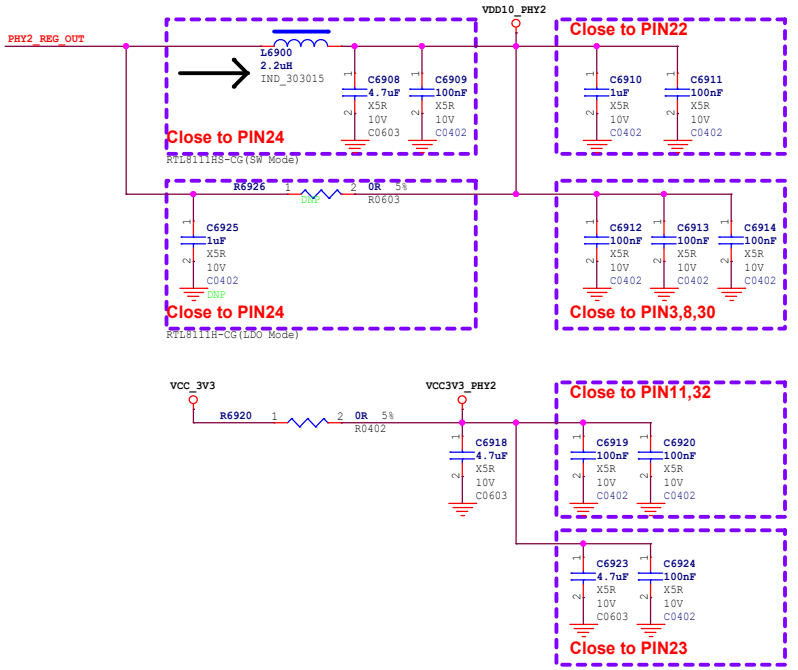






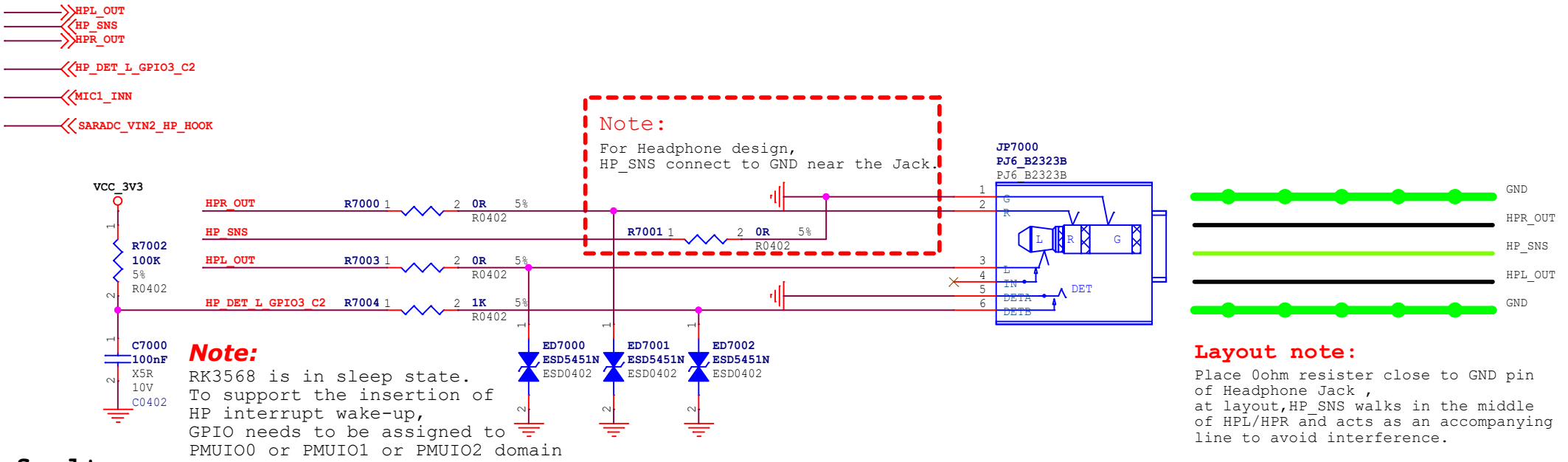






Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	69.Ethernet-PCIE Ethernet				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	54 of 72

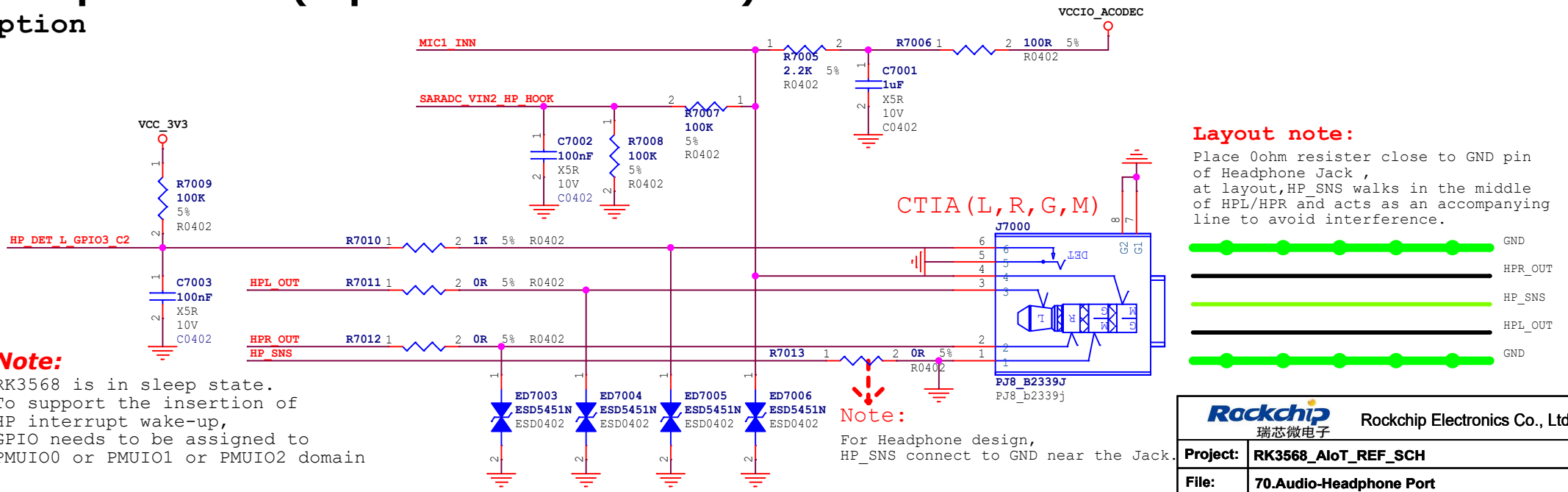


Default

Headphone Jack(3-pole with DET)

Headphone Jack(4-pole with DET & MIC)

Option

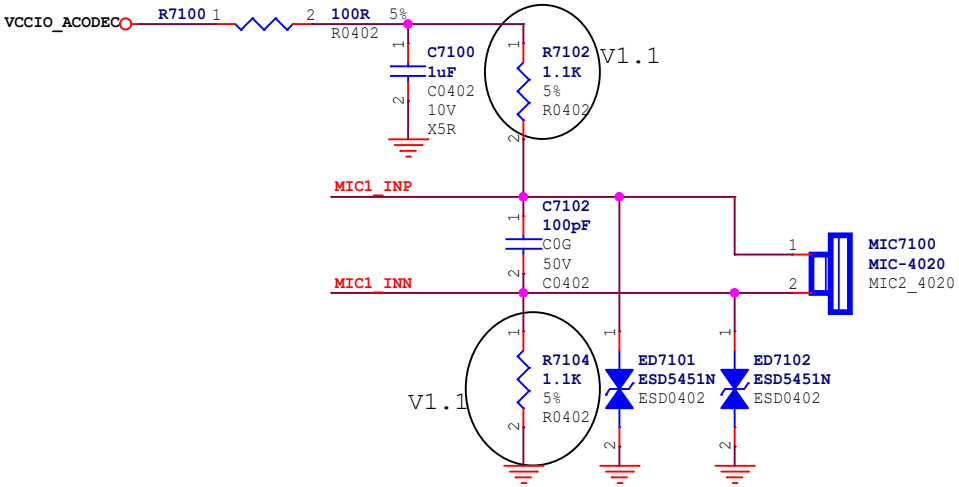


Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	70.Audio-Headphone Port				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	55 of 72

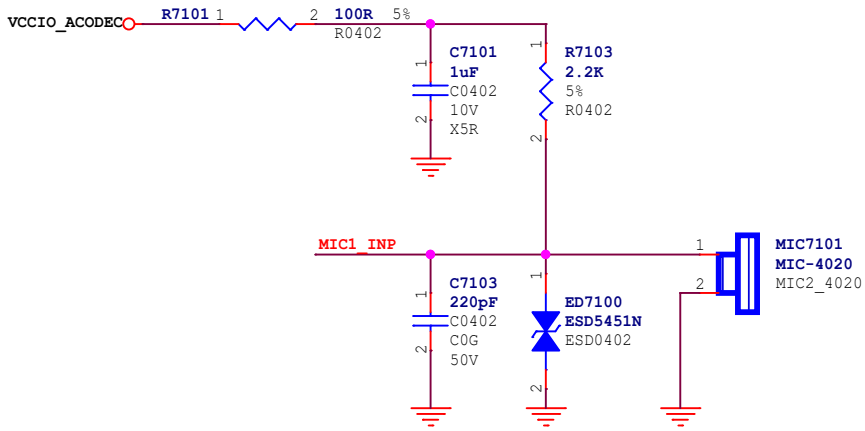
SPKN_OUT
SPKP_OUT

MIC1_INP
MIC1_INN

Default
MIC for 3-pole Headphone Jack

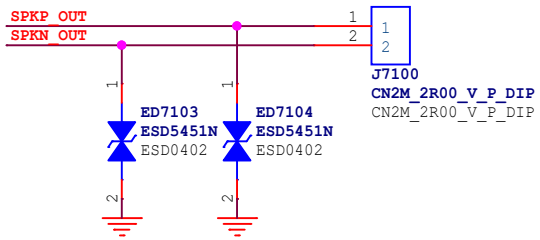


Option
MIC for 4-pole Headphone Jack



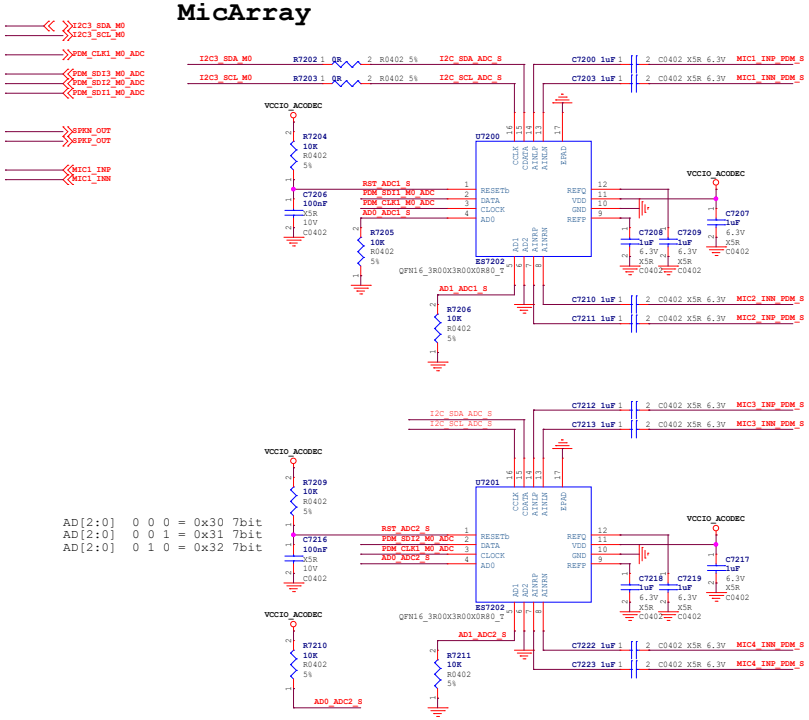
SPK

Note:8ohm/1.3W
Speaker Output

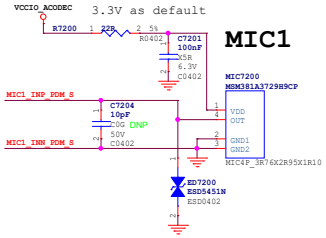


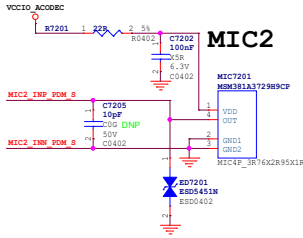
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	71.Audio-SingleMic+RK809_SPK				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	56 of 72

MicArray

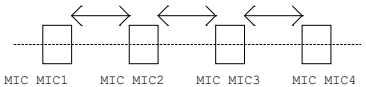


AD[2:0] 0 0 0 = 0x30 7bit
AD[2:0] 0 0 1 = 0x31 7bit
AD[2:0] 0 1 0 = 0x32 7bit



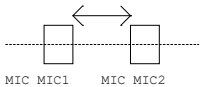


Equal spacing arrangement; according to mic algorithm

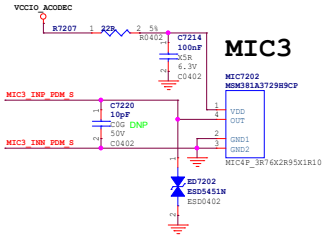


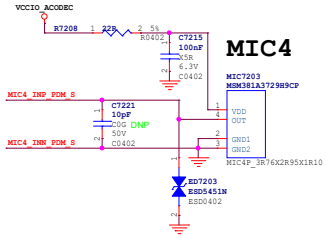
For 4MIC Array Applications

Equal spacing arrangement; according to mic algorithm



For 2MIC Array Applications

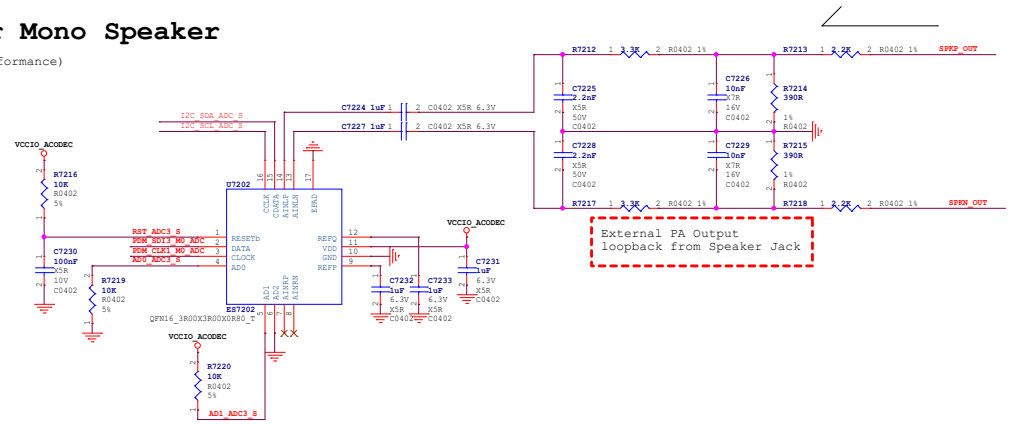




Option1

Loopback for Mono Speaker

(External ADC, better performance)

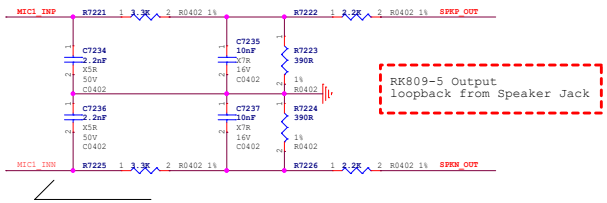


Option2

Loopback for Mono Speaker

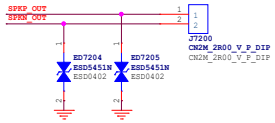
(Available while No MIC is connected to RK809-5)

(cost-effective)



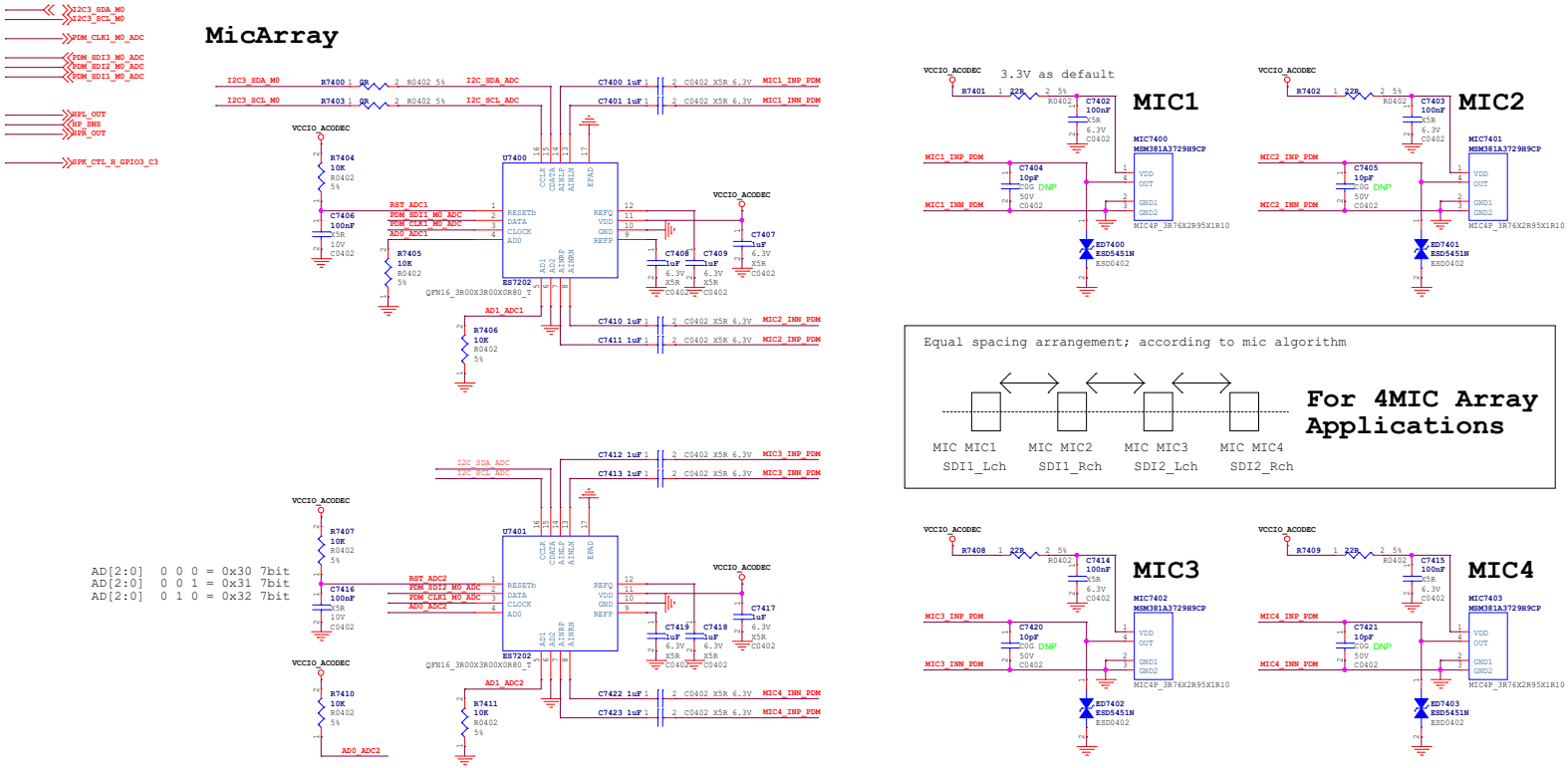
RK809-5 SPK

Note:8ohm/1.3W
Speaker Output



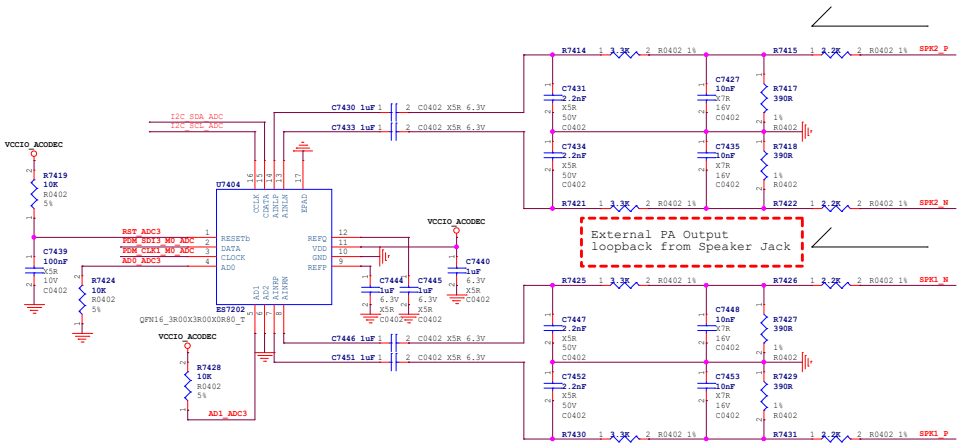
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	72.Audio-MicArray+RK809_SPK		
Date:	Wednesday, June 16, 2021	Rev:	V1.1
Designed by: Zhangtz	Reviewed by: Default	Sheet:	57 of 72

MicArray



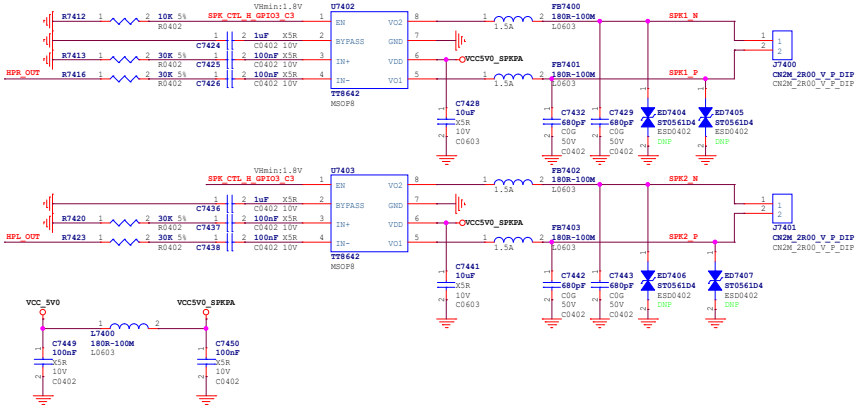
AD[2:0] 0 0 0 = 0x30 7bit
AD[2:0] 0 0 1 = 0x31 7bit
AD[2:0] 0 1 0 = 0x32 7bit

Loopback for Dual Speakers

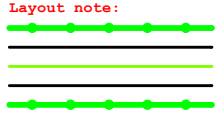


Speaker Output

Note:4ohm/3W



Layout note:



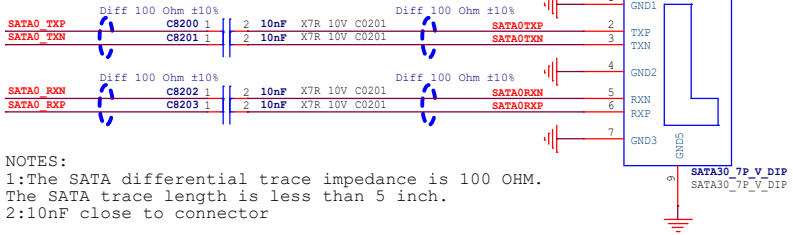
For NO Headphone design,
HP_SNS connect to GND near the PMIC.

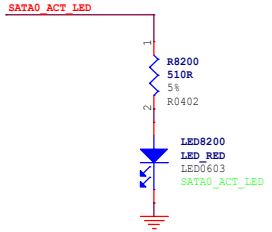
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	74.Audio-MicArray+EXT Dual_SPK		
Date:	Wednesday, June 16, 2021	Rev:	V1.1
Designed by: Zhangtz	Reviewed by: Default	Sheet:	58 of 72

SATA0_TXP
SATA0_TXN
SATA0_RXP
SATA0_RXN
SATA1_TXP
SATA1_TXN
SATA1_RXP
SATA1_RXN
SATA2_TXP
SATA2_TXN
SATA2_RXP
SATA2_RXN
SATA0_ACT_LED
SATA1_ACT_LED
SATA2_ACT_LED

SATA3.0 Port0 Option

And USB3 OTG0 option, Can support SATA0+USB2 OTG0

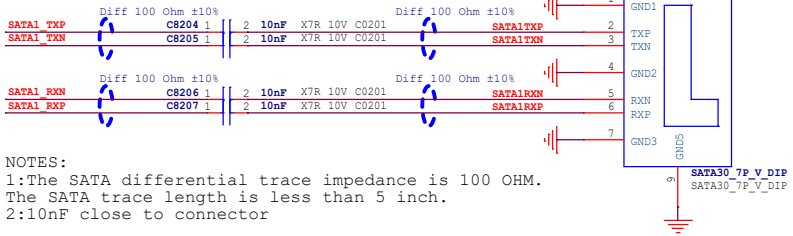


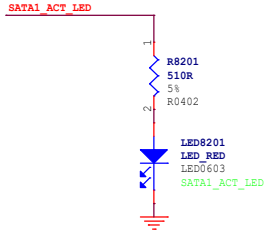


NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA3.0 Port1 Option

And USB3 HOST1 option, Can support SATA1+USB2 HOST1

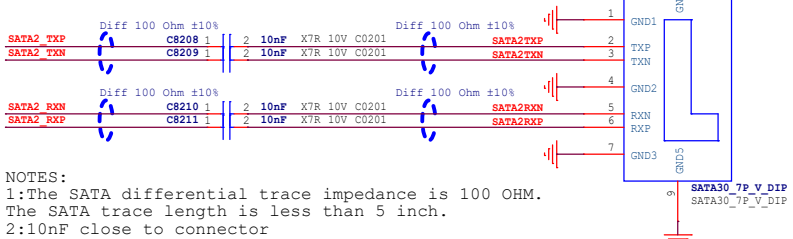


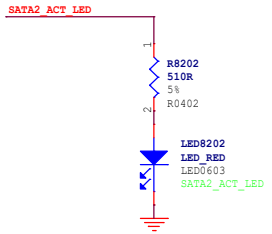


NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA3.0 Port2

And PCIe2.0 option

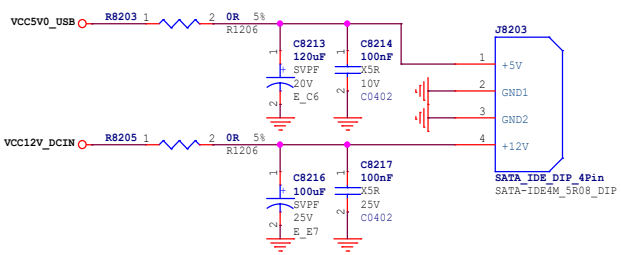


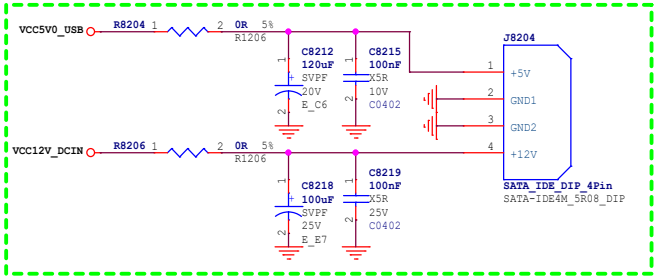


NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

SATA Power

The current is estimated according to the actual number of SATA
High power switching separate power supply is recommended for more than 2

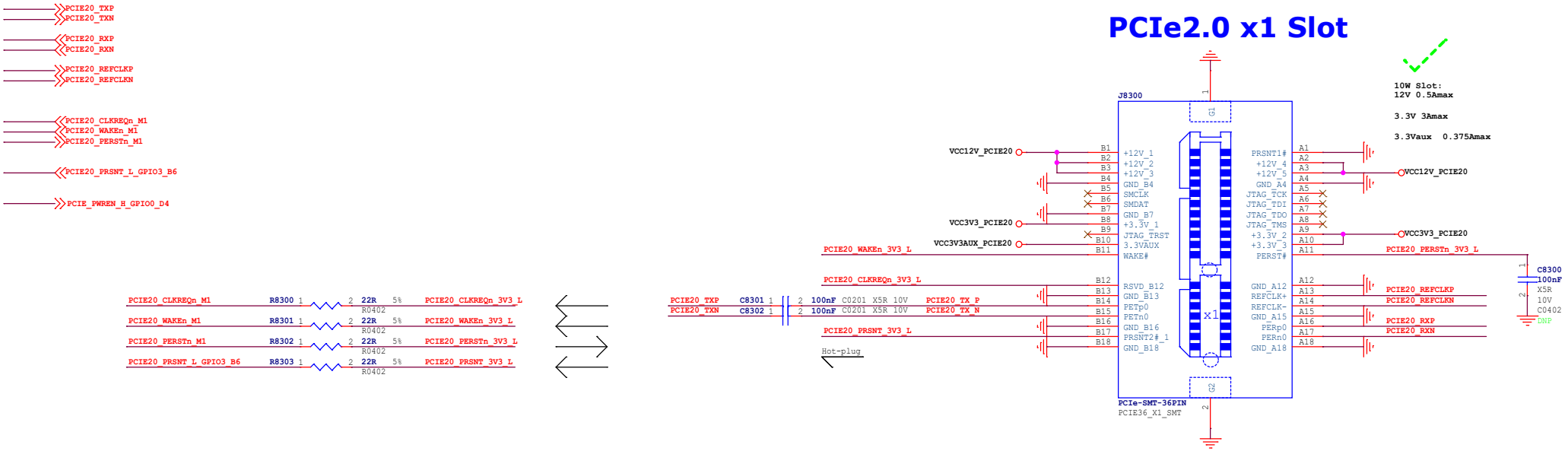


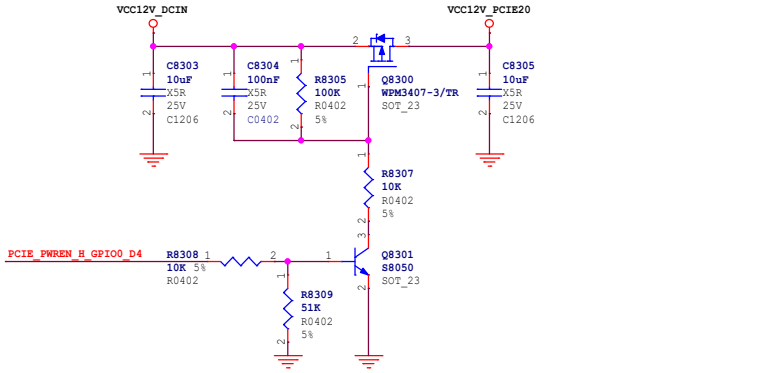


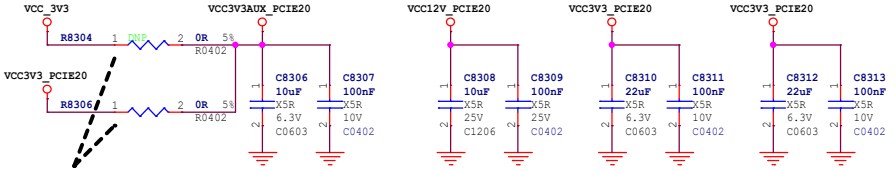
Option

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	82.SATA-SATA3.0 Slot_7P				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	59 of 72

PCIe2.0 x1 Slot

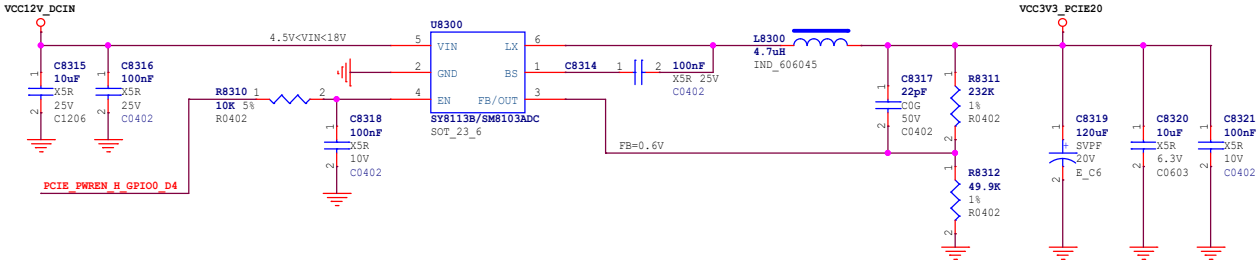






Note:

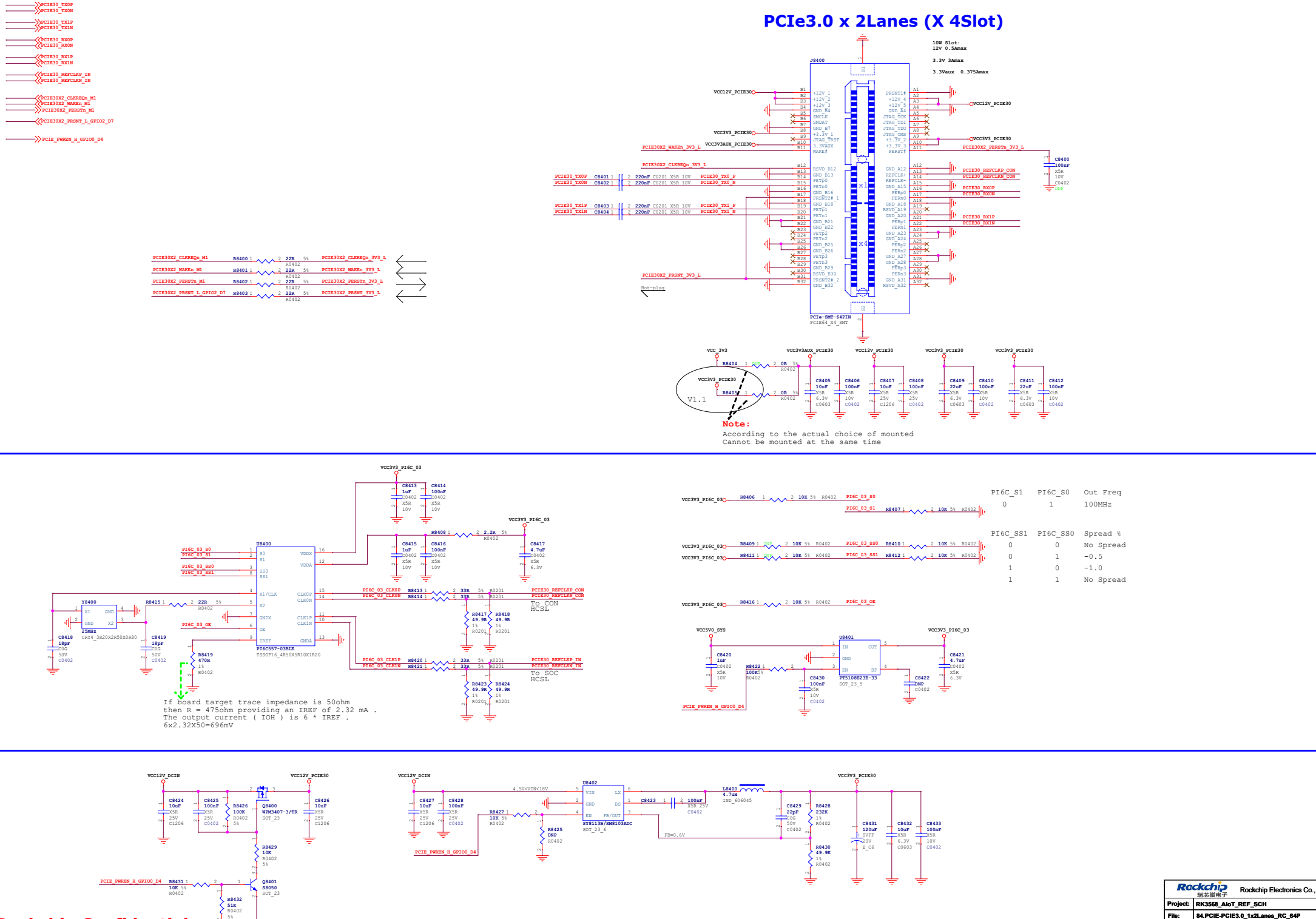
According to the actual choice of mounted
Cannot be mounted at the same time



Rockchip Electronics Co., Ltd
瑞芯微电子

Project:	RK3568_AIoT_REF_SCH				
File:	83.PCIE-PCIE2.0_1x1Lane_RC_36P				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	60 of 72

PCIe3.0 x 2Lanes (X 4Slot)



Note:
According to the actual choice of mounted
Cannot be mounted at the same time

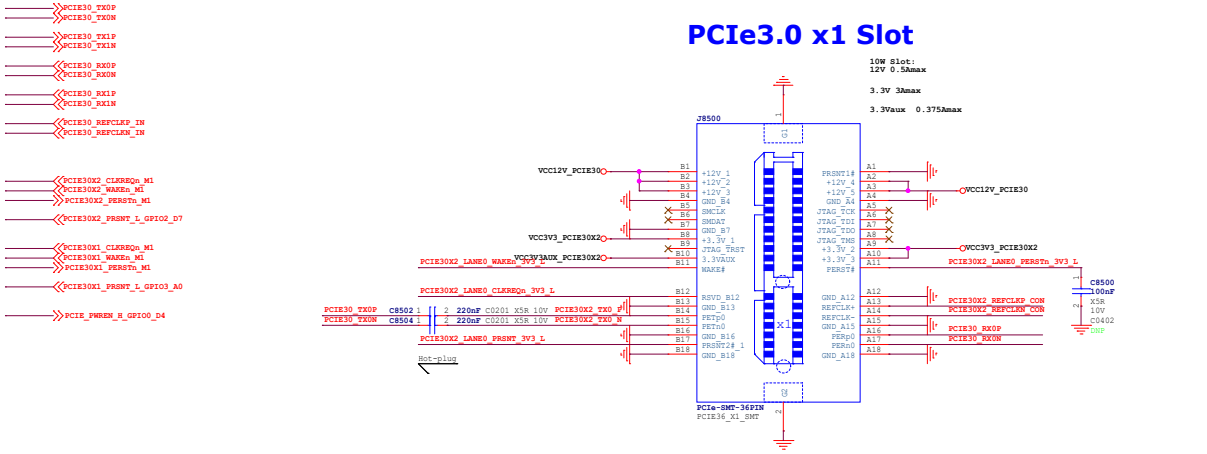
If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA .
The output current (IOH) is 6 * IREF .
6x2.32X50=696mV

PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

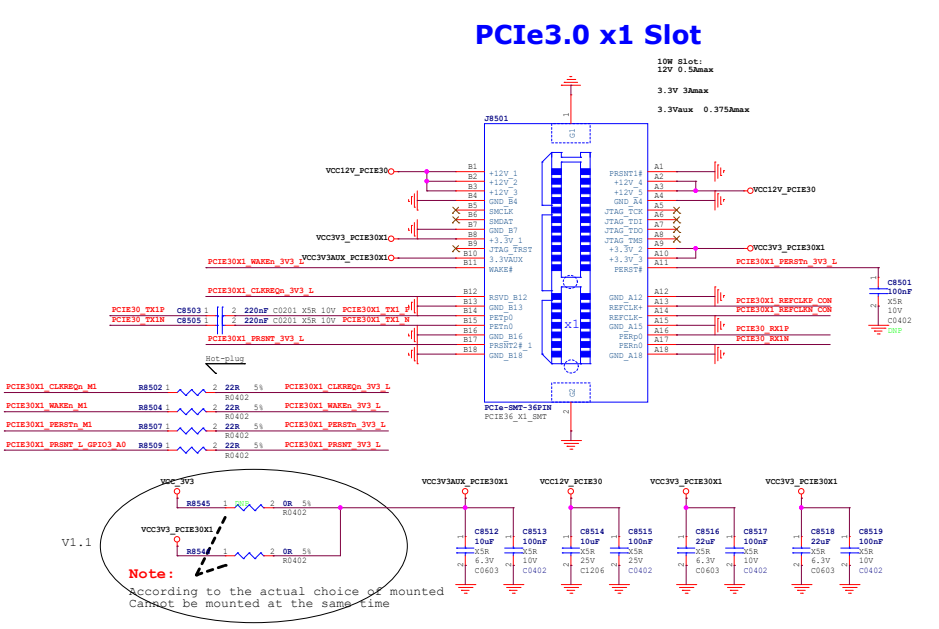
PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread

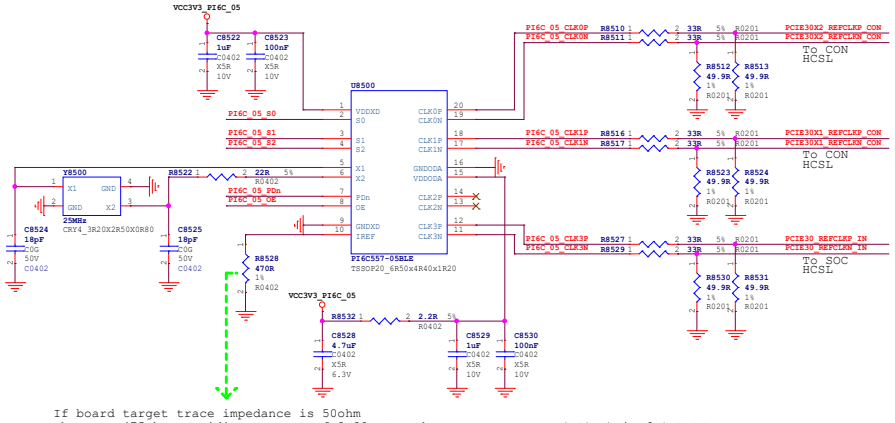
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd
Project:	RK3568_AIoT_REF_SCH
File:	84.PCIE-PCIE3.0_1x2Lanes_RC_64P
Date:	Wednesday, June 16, 2021
Rev:	V1.1
Designed by:	Zhangtz
Reviewed by:	Default
Sheet:	61 of 72

PCIe3.0 x1 Slot

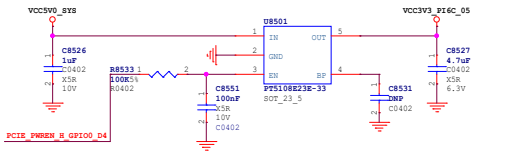


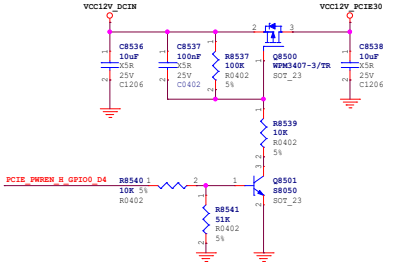
PCIe3.0 x1 Slot

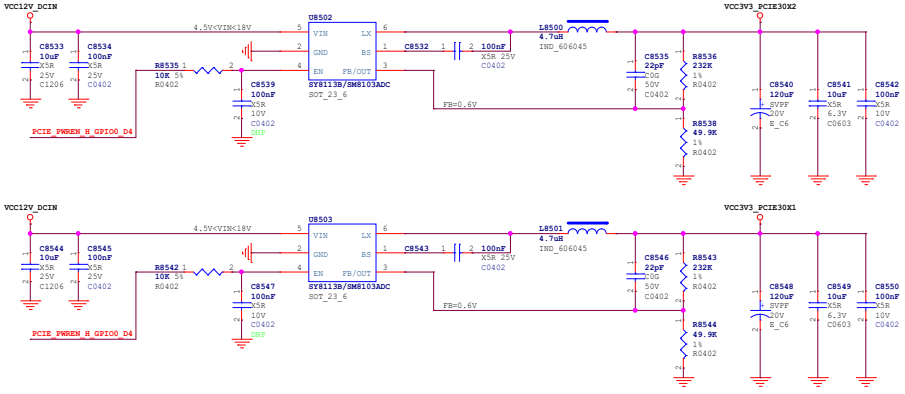




PI6C_S2	PI6C_S1	PI6C_S0	Spread %	Out Freq
0	0	0	-0.5	100MHz
0	0	1	-1.0	100MHz
0	1	0	-1.5	100MHz
0	1	1	No Spread	100MHz







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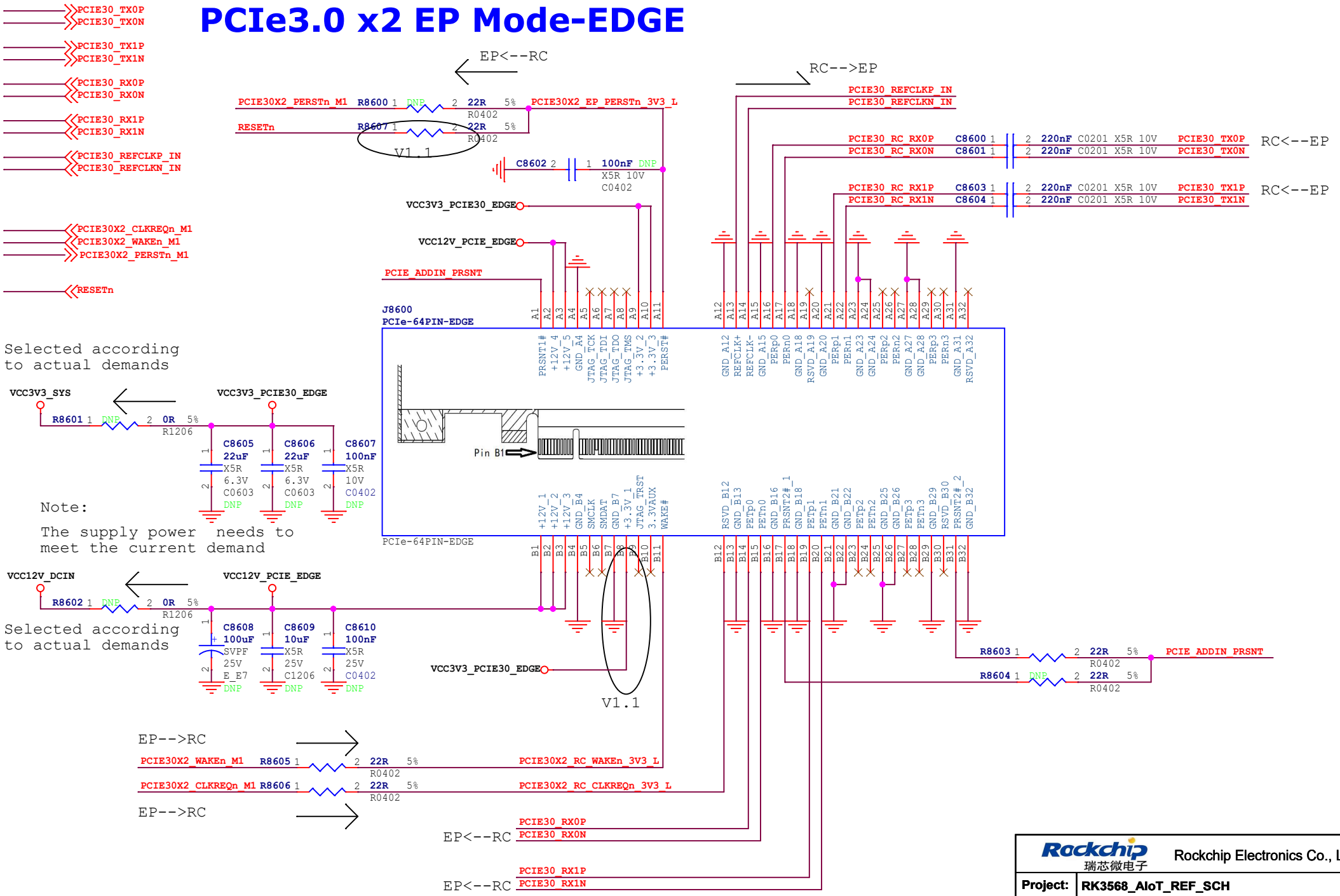
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd		
Project:	RK3568_AIoT_REF_SCH		
File:	85.PCIE-PCIE3.0_2x1Lane_RC_32P		
Date:	Wednesday, June 16, 2021	Rev:	V1.1
Designed by: Zhangtz	Reviewed by: Default	Sheet:	62 of 72

PCIe3.0 x2 EP Mode-EDGE



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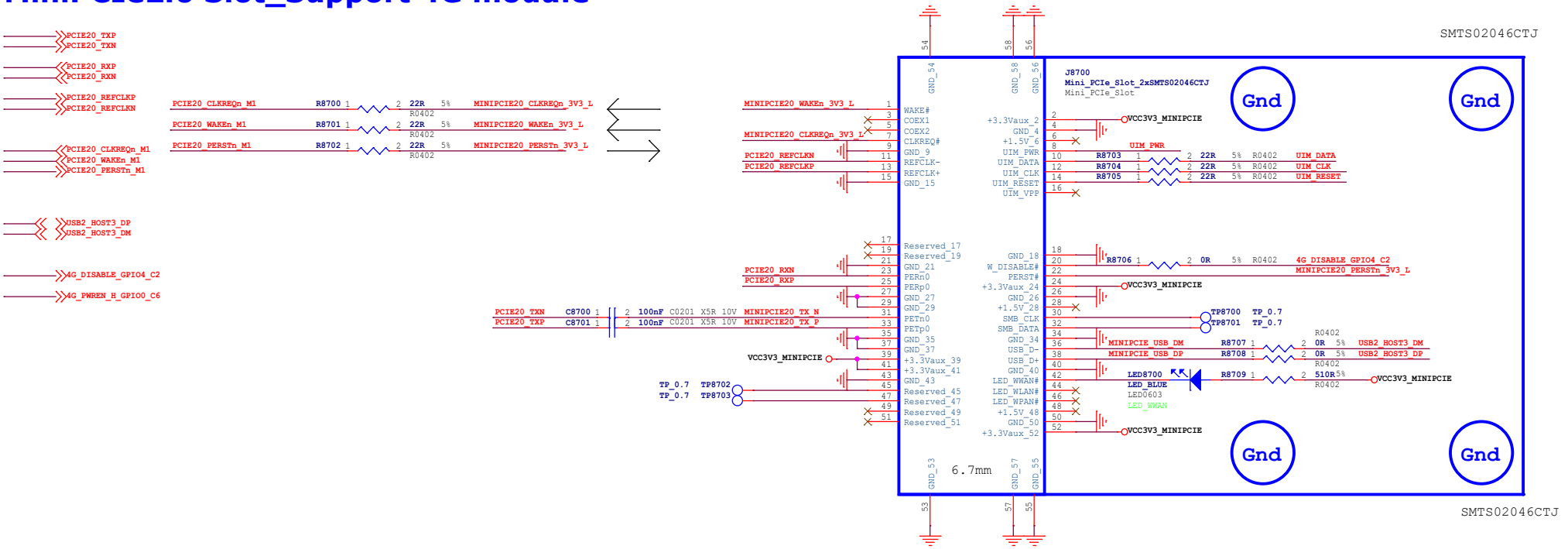
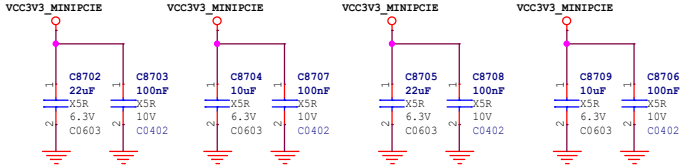
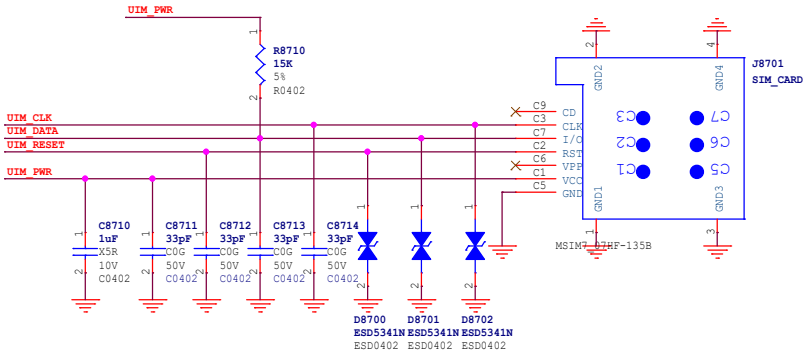
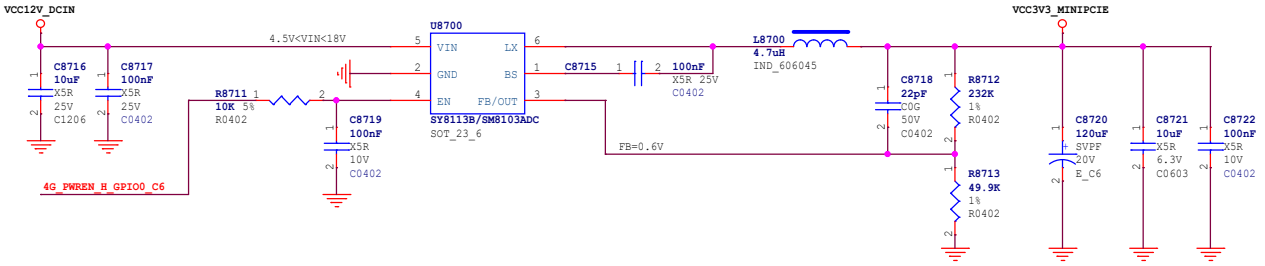
Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	86.PCIE-PCIE3.0_1x2Lanes_EP_64P				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	63 of 72

MiniPCIe2.0 Slot_Support 4G module



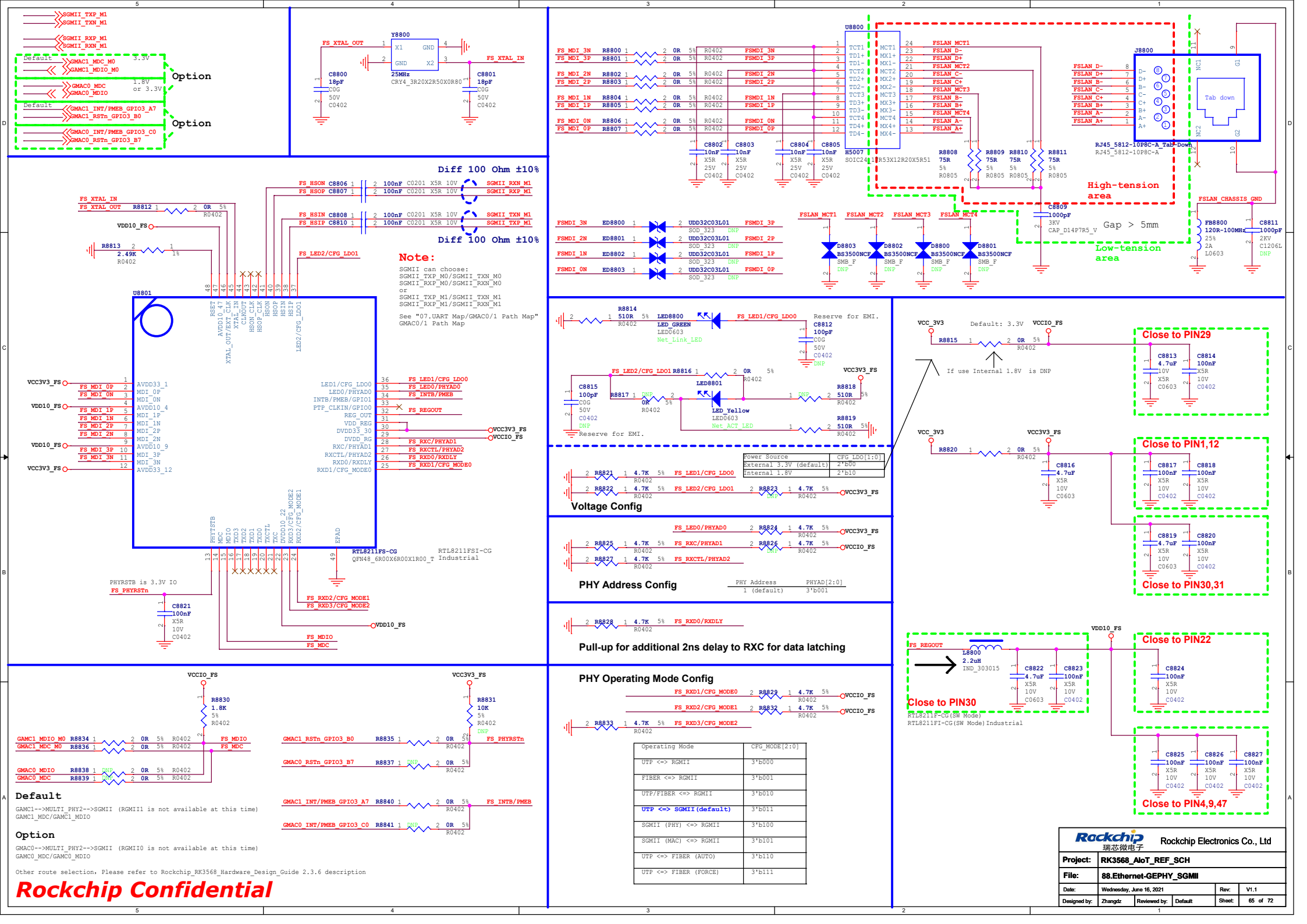






Rockchip Confidential

Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	87.MiniPCIe2.0 Slot_With 4G Fun				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	64 of 72


SGMII_TXP_M1
SGMII_TXN_M1
SGMII_RXP_M1
SGMII_RXN_M1
Default
GMAC1_MDC_M0
GAMC1_MDIO_M0
3.3V
1.8V or 3.3V
Option
GMAC0_MDC
GMAC0_MDIO
Default
GMAC1_INT/PMEB_GPIO3_A7
GMAC1_RSTn_GPIO3_B0
Option
GMAC0_INT/PMEB_GPIO3_C0
GMAC0_RSTn_GPIO3_B7
Y8800
FS_XTAL_OUT
FS_XTAL_IN
25MHz
CRY4_3R20X2R50X0R80
C8800 18pF C0G 50V C0402
C8801 18pF C0G 50V C0402
U8800
FS_MDI_3N R8800
FS_MDI_3P R8801
FS_MDI_2N R8802
FS_MDI_2P R8803
FS_MDI_1N R8804
FS_MDI_1P R8805
FS_MDI_0N R8806
FS_MDI_0P R8807
0R 5% R0402
FSMDI_3N
FSMDI_3P
FSMDI_2N
FSMDI_2P
FSMDI_1N
FSMDI_1P
FSMDI_0N
FSMDI_0P
C8802 C8803 C8804 C8805 10nF X5R 25V C0402
H5007 SOIC24_11R53X12R20X5R51
FSLAN_MCT1
FSLAN_D-
FSLAN_D+
FSLAN_C-
FSLAN_C+
FSLAN_B-
FSLAN_B+
FSLAN_A-
FSLAN_A+
FSLAN_MCT2
FSLAN_MCT3
FSLAN_MCT4
R8808 R8809 R8810 R8811 75R 5% R0805
High-tension area
J8800
RJ45_5812-10P8C-A_Tab-Down
RJ45_5812-10P8C-A
Tab down
FSLAN_CHASSIS_GND
FB8800 120R-100MHz 25% 2A L0603
C8811 1000pF 2KV C1206L DNP
C8809 1000pF 3KV CAP_D14P7R5_V
Gap > 5mm
Low-tension area
ED8800 ED8801 ED8802 ED8803 UDD32C03L01 SOD_323 DNP
D8803 D8802 D8800 D8801 BS3500NCE SMB_F DNP
Diff 100 Ohm ±10%
FS_HSON C8806 FS_HSOP C8807 100nF C0201 X5R 10V
SGMII_RXN_M1
SGMII_RXP_M1
FS_HSIN C8808 FS_HSIP C8810 100nF C0201 X5R 10V
SGMII_TXN_M1
SGMII_TXP_M1
Diff 100 Ohm ±10%
FS_XTAL_IN
FS_XTAL_OUT
R8812 0R R0402
VDD10_FS
R8813 2.49K 1% R0402
FS_LED2/CFG_LDO1
Note:
SGMII can choose:
SGMII_TXP_M0/SGMII_TXN_M0
SGMII_RXP_M0/SGMII_RXN_M0
or
SGMII_TXP_M1/SGMII_TXN_M1
SGMII_RXP_M1/SGMII_RXN_M1
See "07.UART Map/GMAC0/1 Path Map"
GMAC0/1 Path Map
U8801
RSET XTAL_OUT/EXT_CLK XTAL_IN CLKOUT HSON_CLK HSOP_CLK HSON HSOP HSIN HSIP LED2/CFG_LDO1
VCC3V3_FS
VDD10_FS
FS_MDI_0P FS_MDI_0N FS_MDI_1P FS_MDI_1N FS_MDI_2P FS_MDI_2N FS_MDI_3P FS_MDI_3N
AVDD33_1 MDI_0P MDI_0N AVDD10_4 MDI_1P MDI_1N MDI_2P MDI_2N AVDD10_9 MDI_3P MDI_3N AVDD33_12
LED1/CFG_LDO0 LED0/PHYAD0 INTB/PMEB/GPIO1 PTP_CLKIN/GPIO0 REG_OUT VDD_REG DVDD33_30 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/CFG_MODE0
FS_LED1/CFG_LDO0 FS_LED0/PHYAD0 FS_INTB/PMEB FS_REGOUT FS_RXC/PHYAD1 FS_RXCTL/PHYAD2 FS_RXD0/RXDLY FS_RXD1/CFG_MODE0
VCC3V3_FS VCCIO_FS
PHYSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC DVDD10_22 RXD3/CFG_MODE2 RXD2/CFG_MODE1
EPAD
RTL8211FS-CG QFN48_6R00X6R00X1R00_T
RTL8211FSI-CG Industrial
PHYRSTB is 3.3V IO
FS_PHYRSTn
C8821 100nF X5R 10V C0402
FS_RXD2/CFG_MODE1
FS_RXD3/CFG_MODE2
VDD10_FS
FS_MDIO
FS_MDC
R8814 510R 5% R0402
LED8800 LED_GREEN LED0603 Net_Link_LED
FS_LED1/CFG_LDO0
Reserve for EMI.
C8812 100pF C0G 50V C0402 DNP
FS_LED2/CFG_LDO1 R8816 0R R0402
C8815 100pF C0G 50V C0402 DNP
R8817 DNP 0R R0402
LED8801
LED_Yellow LED0603 Net_ACT_LED
R8818 510R R0402
R8819 510R R0402
Reserve for EMI.
Power Source | CFG_LDO[1:0]
External 3.3V (default) | 2'b00
Internal 1.8V | 2'b10
R8821 4.7K R0402 FS_LED1/CFG_LDO0
R8822 4.7K R0402 FS_LED2/CFG_LDO1
R8823 DNP 4.7K R0402 VCC3V3_FS
Voltage Config
FS_LED0/PHYAD0 R8824 4.7K R0402 VCC3V3_FS
FS_RXC/PHYAD1 R8826 DNP 4.7K R0402 VCCIO_FS
R8825 4.7K R0402 FS_RXCTL/PHYAD2
R8827 4.7K R0402
PHY Address Config
PHY Address | PHYAD[2:0]
1 (default) | 3'b001
R8828 4.7K R0402 FS_RXD0/RXDLY
Pull-up for additional 2ns delay to RXC for data latching
PHY Operating Mode Config
FS_RXD1/CFG_MODE0 R8829 4.7K R0402 VCCIO_FS
FS_RXD2/CFG_MODE1 R8832 4.7K R0402 VCCIO_FS
R8833 4.7K R0402 FS_RXD3/CFG_MODE2
Operating Mode | CFG_MODE[2:0]
UTP <=> RGMII | 3'b000
FIBER <=> RGMII | 3'b001
UTP/FIBER <=> RGMII | 3'b010
UTP <=> SGMII (default) | 3'b011
SGMII (PHY) <=> RGMII | 3'b100
SGMII (MAC) <=> RGMII | 3'b101
UTP <=> FIBER (AUTO) | 3'b110
UTP <=> FIBER (FORCE) | 3'b111
VCC_3V3
Default: 3.3V
VCCIO_FS
R8815 0R R0402
If use Internal 1.8V is DNP
C8813 4.7uF 10V X5R C0603
C8814 100nF X5R 10V C0402
Close to PIN29
VCC_3V3
VCC3V3_FS
R8820 0R R0402
C8816 4.7uF X5R 10V C0603
C8817 100nF X5R 10V C0402
C8818 100nF X5R 10V C0402
Close to PIN1,12
C8819 4.7uF X5R 10V C0603
C8820 100nF X5R 10V C0402
Close to PIN30,31
VDD10_FS
FS_REGOUT
L8800 2.2uH IND_303015
C8822 4.7uF X5R 10V C0603
C8823 100nF X5R 10V C0402
Close to PIN30
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C8824 100nF X5R 10V C0402
Close to PIN22
C8825 100nF X5R 10V C0402
C8826 100nF X5R 10V C0402
C8827 100nF X5R 10V C0402
Close to PIN4,9,47
VCCIO_FS
R8830 1.8K 5% R0402
VCC3V3_FS
R8831 10K 5% R0402 DNP
GAMC1_MDIO_M0 R8834 0R R0402
GMAC1_MDC_M0 R8836 0R R0402
FS_MDIO
FS_MDC
GMAC0_MDIO R8838 DNP 0R R0402
GMAC0_MDC R8839 DNP 0R R0402
GMAC1_RSTn_GPIO3_B0 R8835 0R R0402
FS_PHYRSTn
GMAC0_RSTn_GPIO3_B7 R8837 DNP 0R R0402
Default
GAMC1-->MULTI_PHY2-->SGMII (RGMII1 is not available at this time)
GAMC1_MDC/GAMC1_MDIO
GMAC1_INT/PMEB_GPIO3_A7 R8840 0R R0402
FS_INTB/PMEB
GMAC0_INT/PMEB_GPIO3_C0 R8841 DNP 0R R0402
Option
GMAC0-->MULTI_PHY2-->SGMII (RGMII0 is not available at this time)
GAMC0_MDC/GAMC0_MDIO
Other route selection, Please refer to Rockchip_RK3568_Hardware_Design_Guide 2.3.6 description
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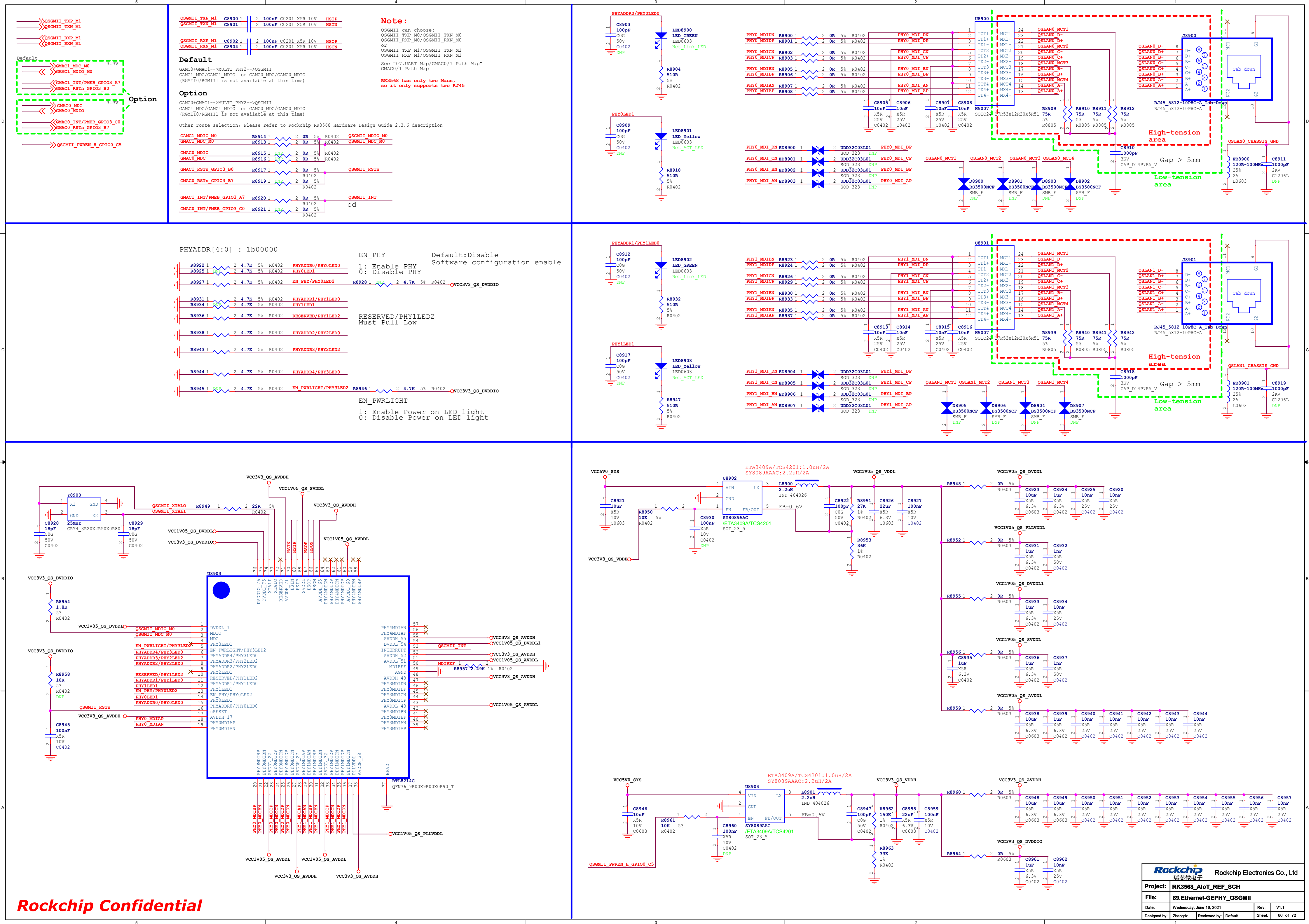
Rockchip Electronics Co., Ltd
Project: RK3568_AIoT_REF_SCH
File: 88.Ethernet-GEPHY_SGMII
Date: Wednesday, June 16, 2021
Rev: V1.1
Designed by: Zhangdz
Reviewed by: Default
Sheet: 65 of 72


Note:
QSGMII can choose:
QSGMII_TXP_M0/QSGMII_TXN_M0
QSGMII_RXP_M0/QSGMII_RXN_M0
or
QSGMII_TXP_M1/QSGMII_TXN_M1
QSGMII_RXP_M1/QSGMII_RXN_M1
See "07.UART Map/GMAC0/1 Path Map"
GMAC0/1 Path Map
RK3568 has only two Macs,
so it only supports two RJ45
Default
GAMC0+GMAC1-->MULTI_PHY2-->QSGMII
GAMC1_MDC/GAMC1_MDIO or GAMC0_MDC/GAMC0_MDIO
(RGMII0/RGMII1 is not available at this time)
Option
GAMC0+GMAC1-->MULTI_PHY2-->QSGMII
GAMC1_MDC/GAMC1_MDIO or GAMC0_MDC/GAMC0_MDIO
(RGMII0/RGMII1 is not available at this time)
Other route selection. Please refer to Rockchip_RK3568_Hardware_Design_Guide 2.3.6 description
PHYADDR[4:0] : 1b00000
EN_PHY
1: Enable PHY
0: Disable PHY
Default:Disable
Software configuration enable
RESERVED/PHY1LED2
Must Pull Low
EN_PWRLIGHT
1: Enable Power on LED light
0: Disable Power on LED light
High-tension area
Low-tension area
Gap > 5mm
Tab down
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
RTL8214C
QFN76_9R00X9R00X0R90_T
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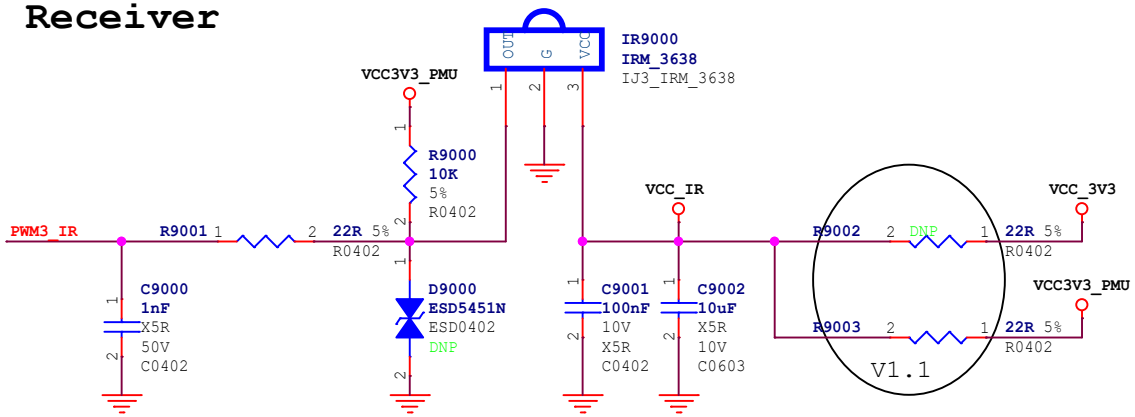
Project: RK3568_AIoT_REF_SCH
File: 89.Ethernet-GEPHY_QSGMII
Date: Wednesday, June 16, 2021
Rev: V1.1
Designed by: Zhangdz
Reviewed by: Default
Sheet: 66 of 72

PWM3_IR

IR Receiver



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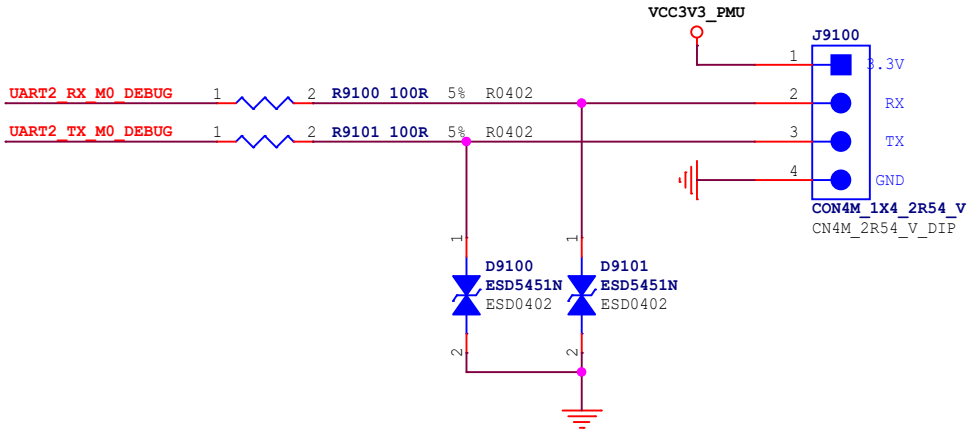
Project:	RK3568_AIoT_REF_SCH				
File:	90.IR Receiver				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	67 of 72

UART2_RX_M0_DEBUG
UART2_TX_M0_DEBUG

Debug UART2



Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	91.Debug UART				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	68 of 72

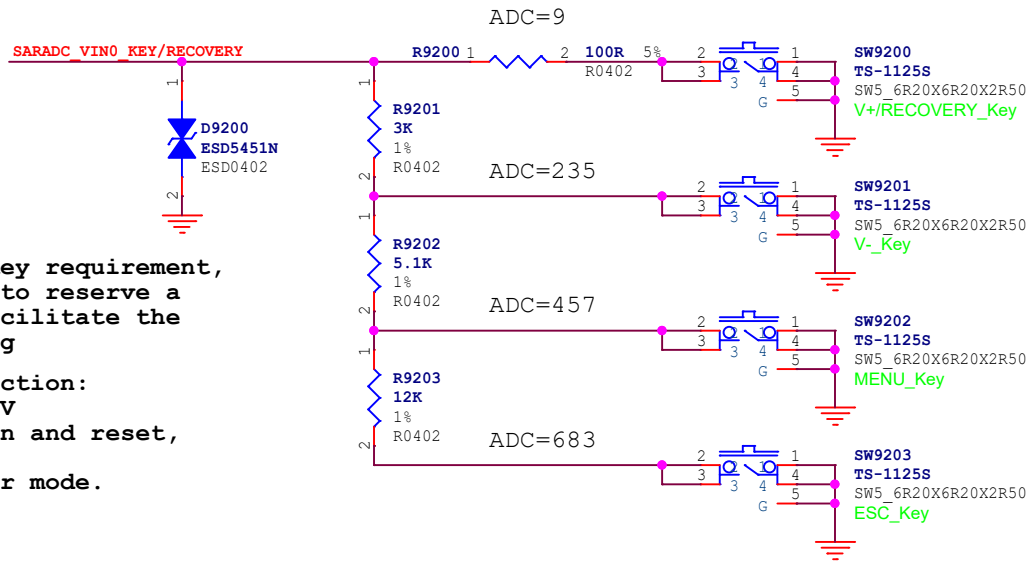
Key Array

SARADC_VIN0_KEY/RECOVERY

SARADC_VIN4
SARADC_VIN5
SARADC_VIN6
SARADC_VIN7

RESETn

RK809_PWRON

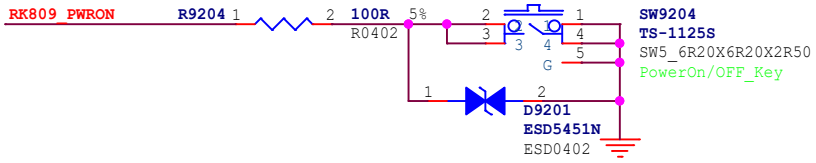


Note:

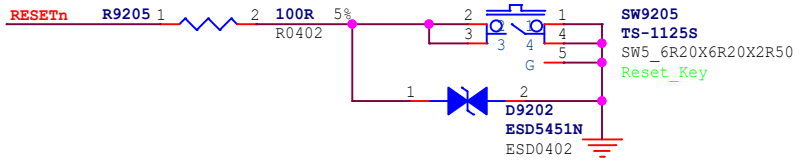
If there is no Key requirement, It is suggested to reserve a SW9200 Key to facilitate the development debug

RECOVERY_Key function:
If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

PowerOn/OFF_Key

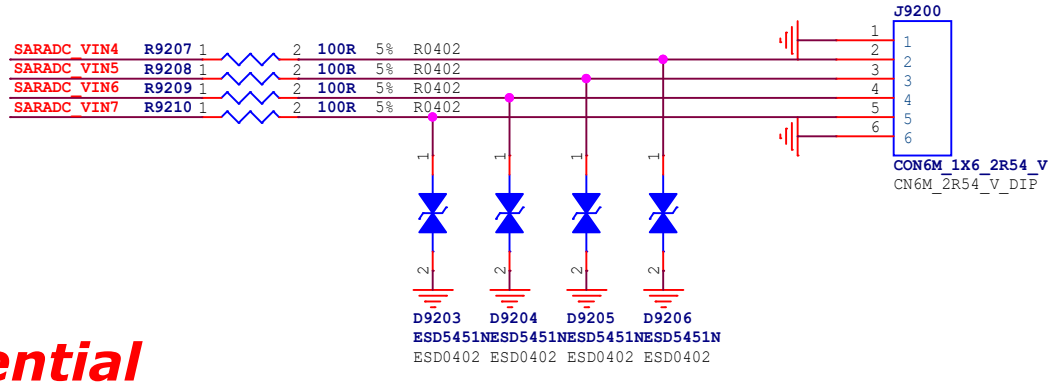


Reset_Key



SARADC

Voltage range:0v-1.8V



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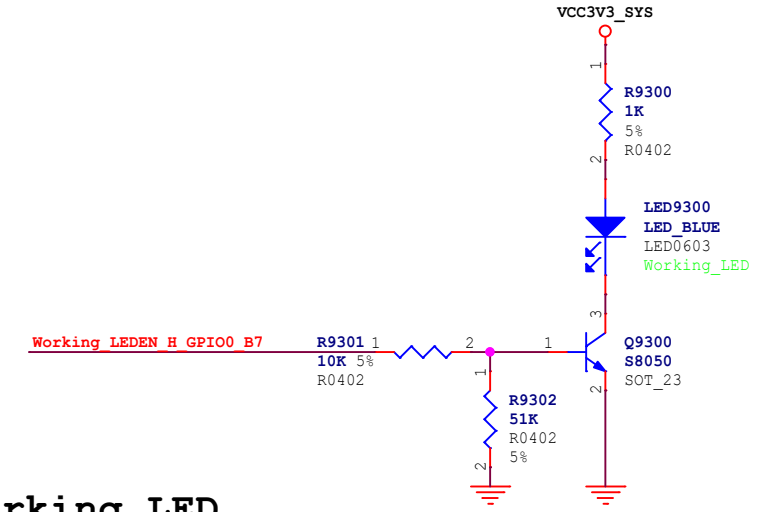
Project:	RK3568_AIoT_REF_SCH				
File:	92.KEY Array/SARADC				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	69 of 72

Working_LEDEN_H_GPIO0_B7

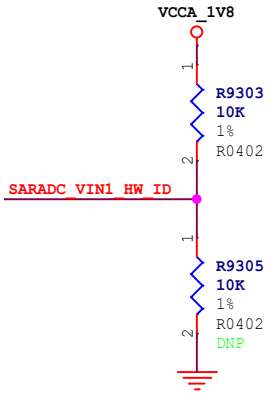
SARADC_VIN1_HW_ID

SARADC_VIN3_BOM_ID



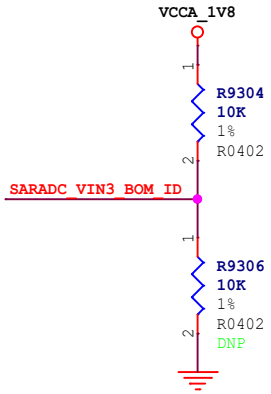
Working LED

HW_ID



SARADC_VIN1	Up Resistance	Down Resistance
HW_ID0	10K	DNP
HW_ID1	10K	110K
HW_ID2	20K	100K
HW_ID3	33K	100K
HW_ID4	18K	36K
HW_ID5	36K	51K
HW_ID6	51K	51K
HW_ID7	51K	36K
HW_ID8	36K	18K
HW_ID9	100K	33K
HW_ID10	100K	20K
HW_ID11	110K	10K
HW_ID12	DNP	10K

BOM_ID



SARADC_VIN3	Up Resistance	Down Resistance
BOM_ID0	10K	DNP
BOM_ID1	10K	110K
BOM_ID2	20K	100K
BOM_ID3	33K	100K
BOM_ID4	18K	36K
BOM_ID5	36K	51K
BOM_ID6	51K	51K
BOM_ID7	51K	36K
BOM_ID8	36K	18K
BOM_ID9	100K	33K
BOM_ID10	100K	20K
BOM_ID11	110K	10K
BOM_ID12	DNP	10K

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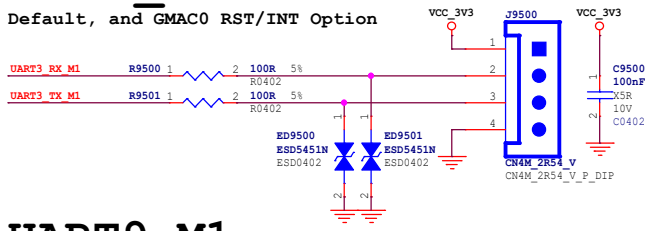
Project:	RK3568_AIoT_REF_SCH				
File:	93.LED/HW_ID/BOM_ID				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	70 of 72

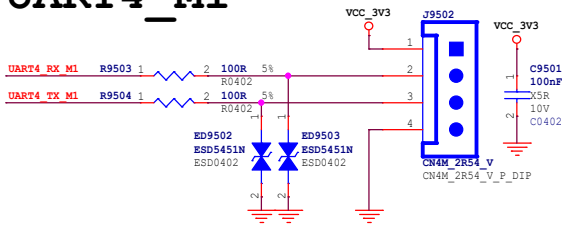
UART9_TX_M1
UART9_RX_M1
UART4_RX_M1
UART4_TX_M1
UART3_TX_M1
UART3_RX_M1
UART7_TX_M1
UART7_RX_M1
RS485_DIR_GPIO3_B5
UART6_TX_M1
UART6_RX_M1
CAN0_TX_M1
CAN0_RX_M1

UART3_M1

Default, and GMAC0 RST/INT Option

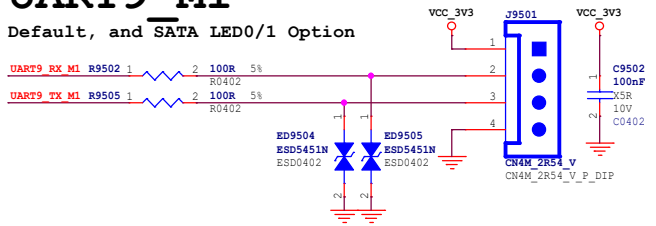


UART4_M1

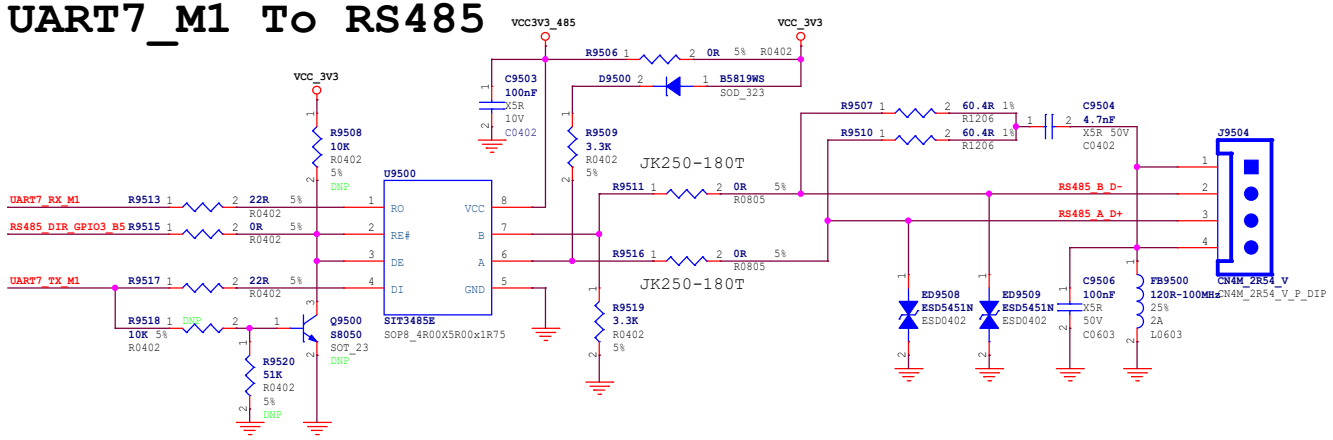


UART9_M1

Default, and SATA LED0/1 Option

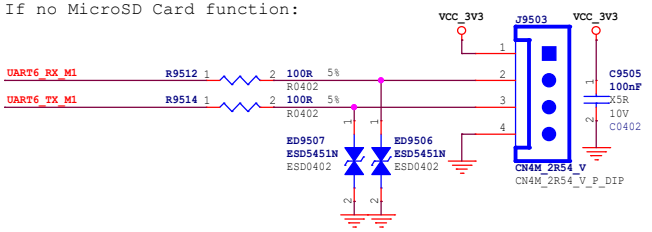


UART7_M1 To RS485



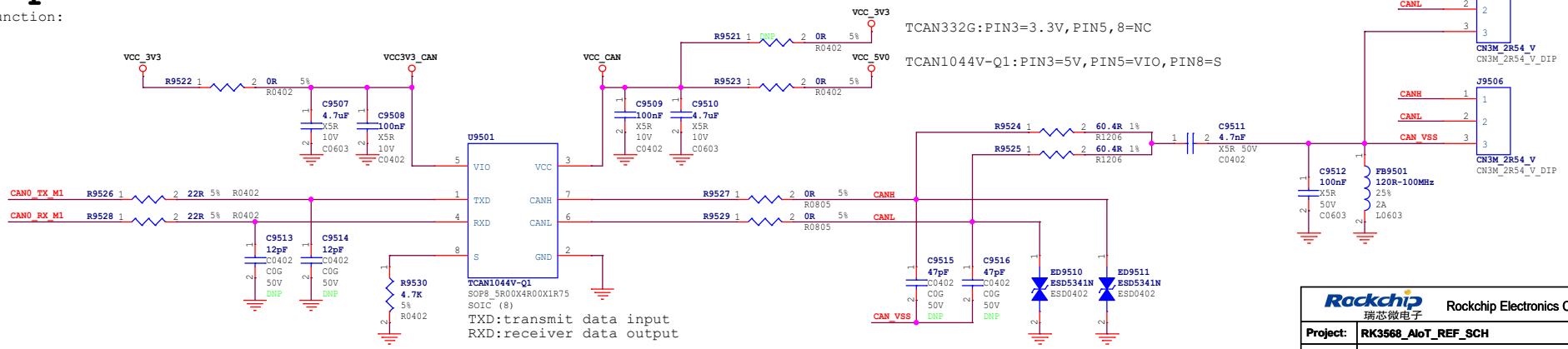
UART6_M1-Option

If no MicroSD Card function:



CAN0_M1-Option

If no MicroSD Card function:



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Project:	RK3568_AIoT_REF_SCH				
File:	95.UART/RS485/CAN Port				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	71 of 72

H9900
HOLE_3R20
HOLE_C3R20_C6R00

H9901
HOLE_3R20
HOLE_C3R20_C6R00

H9902
HOLE_3R20
HOLE_C3R20_C6R00

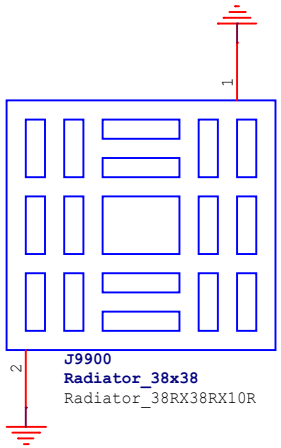
H9903
HOLE_3R20
HOLE_C3R20_C6R00

H9904
HOLE_3R20
HOLE_C3R20_C6R00

H9905
HOLE_3R20
HOLE_C3R20_C6R00

H9906
HOLE_3R20
HOLE_C3R20_C6R00

H9907
HOLE_3R20
HOLE_C3R20_C6R00



J9900
Radiator_38x38
Radiator_38RX38RX10R

TOP Mark

M9900
MARK
MARK

M9901
MARK
MARK

M9902
MARK
MARK

BOTTOM Mark

M9903
MARK
MARK

M9904
MARK
MARK

M9905
MARK
MARK

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Rockchip 瑞芯微电子	Rockchip Electronics Co., Ltd				
Project:	RK3568_AIoT_REF_SCH				
File:	99.Mark/Hole/Heatsink				
Date:	Wednesday, June 16, 2021			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	72 of 72