MTC-20276

Single Chip ISDN NT 2B1Q (INTQ)

Data Sheet

Rev. 2.2 - October 1998

Key Features

- Fully integrated basic rate U to S/T ISDN NT device
- Pin compatible with MTC-20277 INTT (4B3T)
- Full compliance with the applicable ETSI and ITU requirements
- Minimal external components
- < 320mW power consumption, 3.3V operating voltage
- Fully integrated Embedded Operations Channel handling
- Advanced 0.5µ CMOS mixed analog/digital process technology
- -40°C to +85°C or 0 to 70°C operating ranges
- 44 pin PLCC or PQFP

Applications

- Standard ISDN NT1 applications (stand-alone mode)
- Advanced NT with analog line interfaces ("NT1+")
- Micro-PABX
- Data network gateways
- Pair gain systems
- Data terminals
- CTI

General Description

The MTC-20276 INTQ integrates all of the communications functions required in a Basic Rate ISDN Network Terminator on a single monolithic integrated circuit. It provides activation/deactivation on chip and does not require an external microprocessor. The INTQ is designed for the 2B1Q line-code on the U-interface and is pin compatible with the MTC-20277 INTT, which performs identical functions but with the 4B3T U-interface line code. The MTC-20276 includes a GCI expansion port, to allow extended functions to be added (e.g. interfaces to existing analog terminal equipment by means of the MTK-40131 Short-Haul POTS chipset).

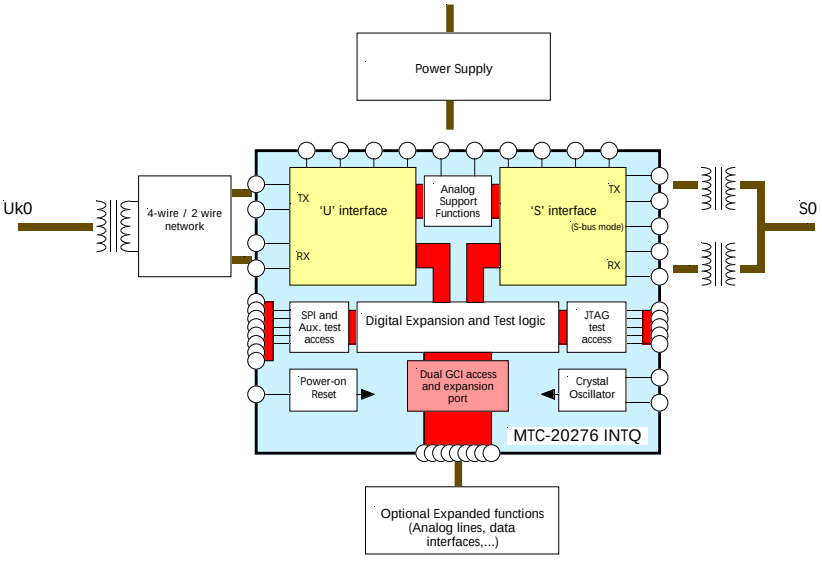

Fig.1: MTC-20276 Application Block Diagram

Ordering Information

Part number	Package	Code	Temp.
MTC-20276PQ-I	44 pin PQFP	PQ44	-40 /+85°C
MTC-20276PC-I	44 pin PLCC	PC44	-40 /+85°C
MTC-20276PQ-C	44 pin PQFP	PQ44	0 /+70°C
MTC-20276PC-C	44 pin PLCC	PC44	0 /+70°C

NT and Extended NT Functions ("NTplus")

The MTC-20276 has a number of test access ports to facilitate system or production testing. One of these ports is configured as a dual GCI interface, which operates in one of two modes. In Mode 0 (GMode = logic 0), the GCI port allows the data flow between the 'U' and the 'S' ports to be optionally monitored.
This is the "stand alone" mode, which is the normal mode for simple NT1 applications. No additional microprocessor or other control device is required in this mode.

Mode 1 (GMode = logic1) allows separate access to the 'U' and the 'S' ports, for use by an external GCI compatible controller device. In this mode, the chip supports additional features required by extended NT modules ("NT1+") such as interfaces to existing analog equipment, or advanced data communication gateways.

The application section describes the circuit configuration of the MTC-20276 in its stand alone mode, for conventional NT1 applications. (Figure 4)

Figure 2 below shows the system concept of an MTC-20276/77 in an "NT1+" application, in combination with the MTK-40131 "SH-POTS" chipset for short-haul analog telephone lines.

MTC-2028xx is one of a family of interface and controller devices which cover a wide range of applications, e.g. MTC-20280for ISDN NT+ or small PABX applications

Standards Compliance

MTC-20276 complies with relevant ANSI and ETSI specifications.

ETSI ETS 300 297
ETSI ETS 300 012
ETSI ETR 80
ANSI T1.601
ITU I.430
ITU G.961

* GCI (General Circuit Interface), is an interface specification developed jointly by Alcatel, Italtel, GPT and Siemens, and can be obtained from Alcatel Microelectronics.

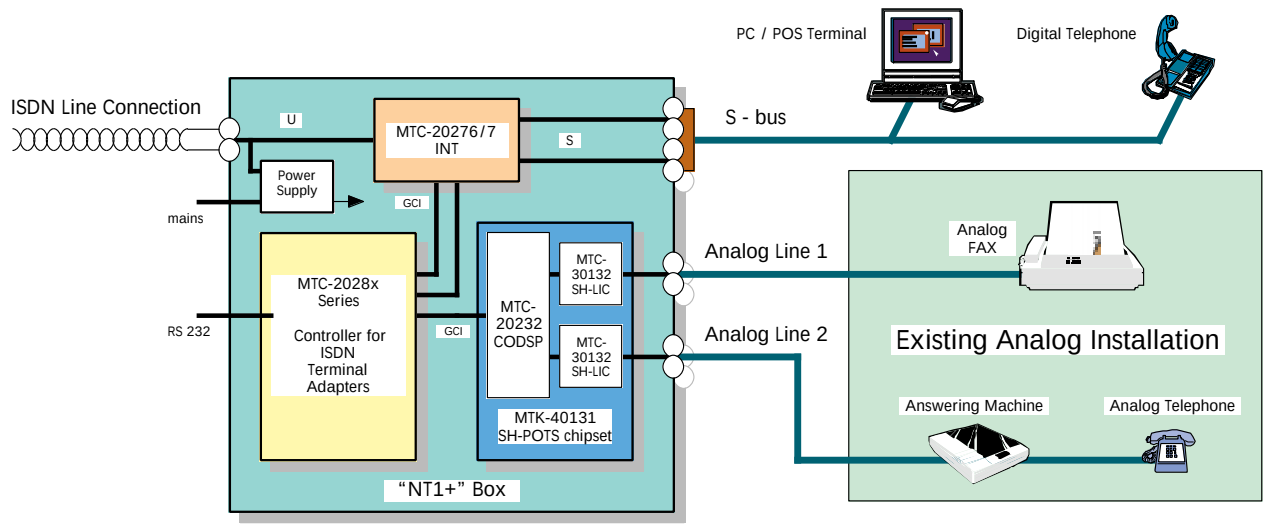

Fig.2: Concept of an NT1+ Configuration for 2 Analog Lines

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S-Interface Programming

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Electrical Characteristics

Absolute Maximum Ratings

Operation of the device beyond these conditions is not guaranteed. Sustained exposure to these limits will adversely effect device reliability.

Table 1

Parameter	Max	Units
DVDD, AVDD	4.8	V (see note)
Vin, Voltage on any device pin	VSS-0.3 VDD+0.3 or 3.63	V V, whichever is lower
Storage temperature	-65 to +150	°C
Temperature under bias	-55 to +125	°C
Lead Temperature (soldering 10 sec)	300	°C

Note: Exposure to voltages at or above this level for more than 10 hours accummulated over the device's operating life will adversely effect reliability.
Note 2. All logic pins except NRESET, which is a Schmitt-trigger input with hysteresis.

Operating Conditions

Unless otherwise stated, the following electrical characteristics are valid over the ranges specified here. (Vss = 0V).

Table 2

Parameter	Min	Max	Units	Note
DVDD, AVDD	3.15	3.45	V	=3.3V ±5%
SN_{AVDD}, supply noise, analog		10	mVpp	
SN_{DVDD}, supply noise, digital		100	mVpp	
SN_{AREF}, supply noise, analog ref.		0.1	mVpp	Note 2
I_{AREF}	- 0.25	+ 0.25	mA	load on AREF Pin
Crystal frequency	15.359	15.361	MHz	±50ppm, Note 1
Temperature range	-40	+85	°C	

Note 1: An external clock may be applied to XTAL2, pin 24. Temperature dependent drift <10ppm.

Note 2: AREF is an output, designed to allow a decoupling capacitor to be placed on the internal analog reference voltage. The external circuit layout must avoid the induction of noise on this pin.

DC Characteristics

Table 3

Parameter	Conditions	Min	Max	Units	Note
P_{tot}	Total power consumption, active		350	mW	1,3
P_{pd}	Power consumption, power-down		20	mW	
VIH	Input level, logic 1	0.8		DVDD	2
VIL	Input level, logic 0		0.2	DVDD	2
VOH	Output level, logic 1	0.85		DVDD	2
VOL	Output level, logic 0		0.4	V	2
V_{IH}	Rising, NRESET	1.7	1.9	V	2
V_{IL}	Falling, NRESET	0.9	1.1	V	2
V_{AREF}	Reference voltage output, load current < ±250µA.	1.6	1.7	V	
V_{TNRES}	Nreset input threshold	1.6	1.7	V	

Note 1: U and S active, random signal. U loaded 135 Ohm, S loaded 50 Ohm.

AVDD (U - PIN 43) = 3.3V
AVDD (S - PIN 36) = 3.0V*
DVDD (PIN 16 & 26) = 3.0V*
* Using 4 Ω resistor to AVDD (PIN 43)

Note 2: All logic pins except NRESET, which is a Schmitt-trigger input with hysteresis.
Note 3: 320 mw typ.

AC Characteristics

Table 4

Parameter	Conditions	Min	Max	Units	Note
Cin	Input capacitance any pin		1	pF	
Cload	Load capacitance on any output pin		100	pF	
V_{TPWRES}	Reset pulse width	10		mS	

Quality / Reliability

Early failure rate	≤ 0.3% at 3000 hours
Long term failure rate	≤ 300 FIT for 45°C average ambient and 45% average humidity
Lifetime	≥ 15 years

Package / Pinout

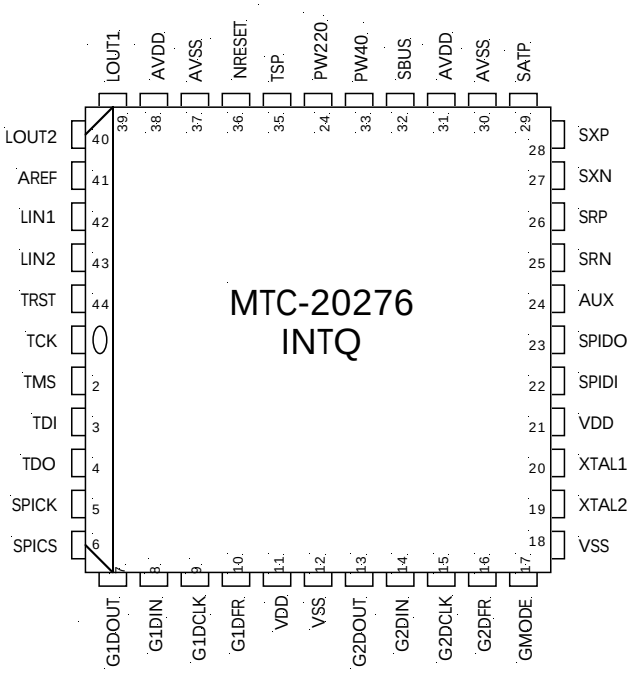


Fig. 3a: Pinout, 44PLCC Package (MTC-20276PC)

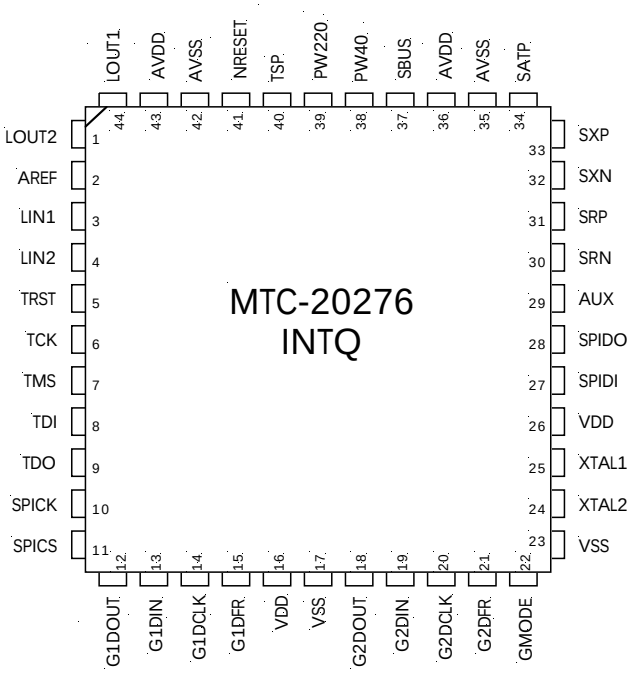


Fig. 3b: Pinout, 44 PQFP Package (MTC-20276PQ)

Pin Description

The table gives a summary of all INTQ pins and their functions.

Table 5

Nr.	Function	Name	Dir.	Description
44		LOUT1	O	U-interface analog outputs. The connections LOUT1 and LOUT2 interface
1		LOUT2	O	the U driver outputs, via termination resistors and the line coupling
	U			transformer, to the U0 reference point.
3		LIN1	I	U-interface analog inputs to the INTQ from the analog 'hybrid'
4		LIN2	I	
2		AREF	O	Analog ground, +1.65 V ±3%. Used as reference voltage for A/D and D/A.
43		AVDD	P	+3.3V ±5% power supply for analog U-interface functions
42		AVSS	P	0V ground for analog U-interface functions
33		SXP	O	S-interface analog outputs. SXP and SXN interface the S-driver outputs
32		SXN	O	via terminating resistors and the Tx line coupling transformer to the S0
				reference point (Tx).
31	S	SRP	I	S-interface analog inputs. SRP and SRN interface the S-inputs via the Rx line
30		SRN	I	coupling transformer to the S0 reference point (Rx).
37		SBUS	I	S-bus type configuration. 1 = short bus with fixed timing, 0 = adaptive
				timing for extended bus or point-to-point
34		SATP	O	Analog test pin. Used for test purposes only, should be left open circuit
36		AVDD	P	+3.3 ±5% power supply for analog S-interface functions
35		AVSS	P	0V ground for analog S-interface functions
12		G1DOUT	O	Primary GCI interface G1:
13		G1DIN	I/O	GMODE = 0 : Monitoring of the internal GCI between the U and S.
14	GCI	G1DCLK	O	GMODE = 1 : NTplus mode; complete GCI connected to U with U as master.
15		G1DFR	O	G1DOUT = data output G1DIN = data input (output direction in monitoring mode) G1DCLK = 512 KHz GCI clock G1DFR = 8KHz GCI frame clock which identifies the beginning of the frame of G1DIN and G1DOUT
18		G2DOUT	O	Secondary GCI interface G2:
19		G2DIN	I	GMODE = 0 : No function
20		G2DCLK	I	GMODE = 1 : NTplus mode; complete GCI connected to S with external master.
21		G2DFR	I	G2DOUT = data output G2DIN = data input G2DCLK = 512KHz GCI clock G2DFR = 8KHz GCI frame clock which identifies the beginning of the frame of G2DIN and G2DOUT Remark : if NT Plus mode is not used, the inputs should be strapped high or low.
22		GMODE	I	Select NTplus mode. 0 = monitoring mode, 1 = NTplus mode.
5		TRST	I	TAP (Test Access Port) controller reset, active low
6	JTAG	TCK	I	TAP controller clock, maximum 10 MHz
7		TMS	I	TAP controller mode selection
8		TDI	I	TAP controller input
9		TDO	O	TAP controller output

41	RESET	NRESET	I	Hardware reset, active low. Schmitt-trigger input for connection to external RC or logic device.
25	OSC.	XTAL1	O	Connection to external crystal (15.36MHz ± 100ppm)
24		XTAL2	I	Connection to external crystal. May also be used as input for external master clock source.
40	Monitor	TSP	I	Transmit Single Pulses. INTQ transmits single pulses of alternating maximum positive and negative polarity at the S and U-interface. Pulse repetition rate is 0.67 kHz at the U-interface, for test purposes and as a search tone on the line.
39		PW220	I	Indicate if the local mains power supply is available. 1 = mains power supply ON 0 = mains power supply OFF
38		PW40	I	Indicate if the local 40V power supply is available. 1 = 40V power supply ON 0 = 40V power supply OFF
10		TEST0	O	Factory use only. Leave open circuit.
11		TEST1	O	
27		OPTO	I	Opto isolator input. See below.
28		LED	O	State indicator LED. See below.
29		CSO	I	Indicate cold-start-only operation mode: 0 = normal mode 1 = cold-start-only operation mode*
16		VDD	P	+3.3 V ±5% power supply for digital functions
26		VDD	P	
17		VSS	P	0V ground for digital functions
23		VSS	P	

* This only affects the "CSO" bit in the upstream M symbol, and does not influence the activation performance of the INTQ.

Device pin 27 (OPTO) is used to determine whether an automatic upstream activation request is performed after power-up or reset, or not. (New releases of the relevant ETSI specifications require automatic activation on power-up, whereas previous releases did not)
Pin 27 should be strapped as follows:

Function:	**Pin 27 strapped to:**
Automatic activation request	VDD
No automatic activation request	VSS

LED Indicator

The LED output can source up to 4mA to directly drive an LED, via a current limiting resistor.

Table 6

LED OFF	Both U and S-interfaces are inactive
Fast flashing (8Hz)	The U-interface is attempting to synchronize, or the EOC has activated a 2B+D loopback.
Slow flashing (1Hz)	The U-interface is synchronized and the S-interface is attempting to synchronize.
LED ON	Both U and S-interfaces are fully synchronized and 'connect through' status is achieved.

Application Information

The MTC-20276 requires very few external components, all of which are low-cost and readily available types. In addition, the use of a 44PQFP package style allows further savings in the total cost and physical size of the ISDN NT module.

The following recommended applications information is constantly being reviewed to improve cost and performance. Please contact Alcatel Microelectronics' application support

NT1 Schematic

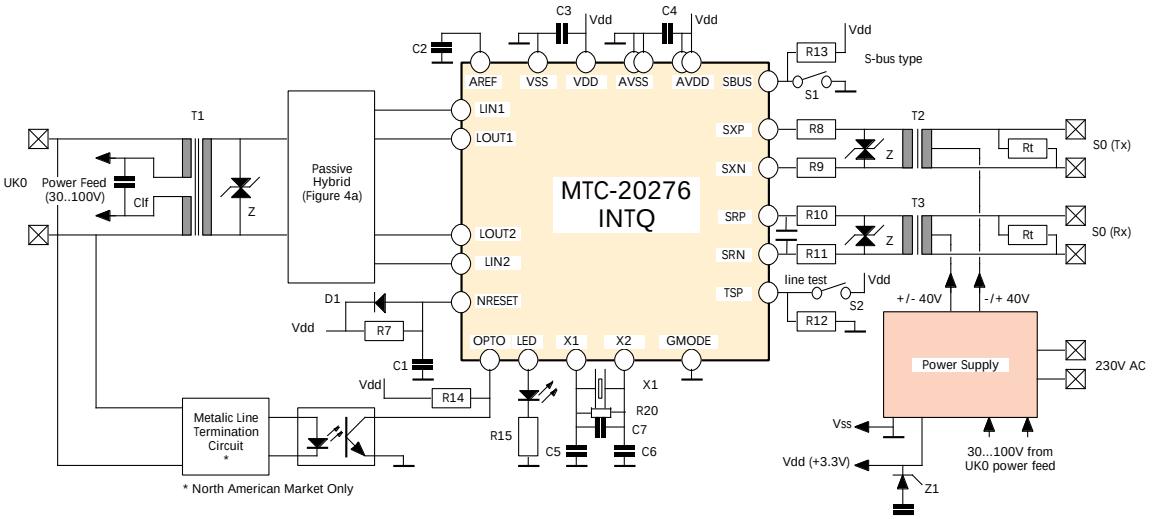


Fig. 4: NT1 Application Schemat-

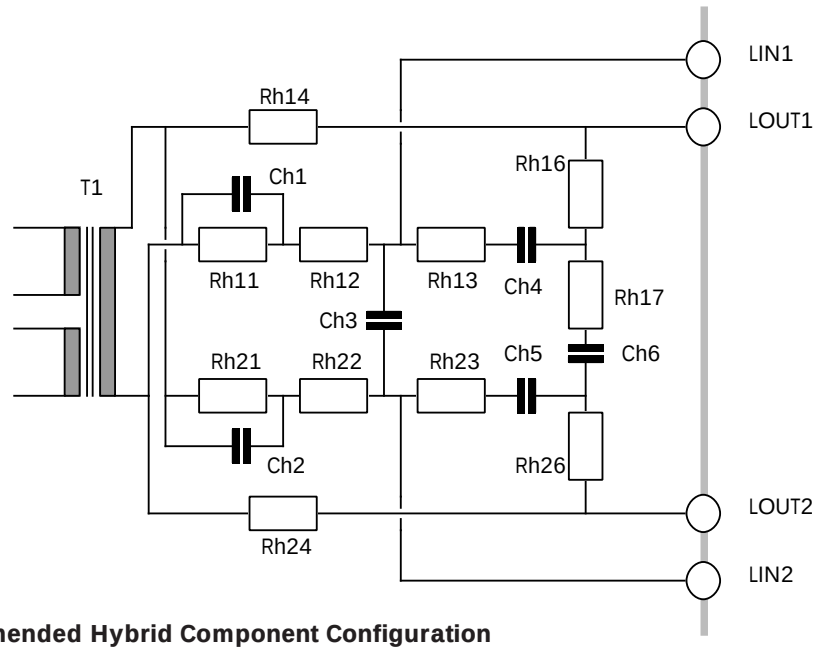


Fig. 4a: Recommended Hybrid Component Configuration

Recommended Component Values

Table 7

Component	Function	Value	Comment
R7,R12,R13,R14	Pull-up / down	100kΩ	
R8,R9	S-bus transmit impedance	30Ω	±1%
R10,R11	S-bus receive impedance	5kΩ	±1%
Rt	S-bus termination resistor	100Ω	
R15	LED current limit	680Ω	-
Rh14, Rh24	U feed bridge	12.3Ω (15Ω / / 68Ω)	±1%
Rh11, Rh21	Hybrid	1k	±1%
Rh12, Rh22	Hybrid	4.33kΩ (56k / / 4.7k)	±1%
Rh13, Rh23	Hybrid	6.8kΩ	±1%
Rh16, Rh26	Hybrid	100Ω	±1%
Rh17	Hybrid	592Ω (720Ω / / 3.3k)	±1%
Rh 18, 19	Hybrid	150Ω	
X1	crystal	15.36 MHz	see text
C1,C2	reset delay	100nF	
C3,C4	supply decoupling	100nF	
C5,C6	crystal load	22pF	see text
C7	crystal load	0 to 22pF (optional)	see text
R20	crystal stabilizer	1mΩ	
Clf	Line-feed coupling	2.2µF	250V
Ch1, Ch2	Hybrid	4n7	
Ch3	Hybrid	470p	
Ch4, Ch5	Hybrid	40n	
Ch6	Hybrid	2n7	
D1	loss-of-power reset	1N4148	any small signal diode
Z1	Power Supply Clamp	4.1V zener	
T1	U transformer	1:2, 15 mH	see text
T2,T3	S transformer	2:1	see text
S1	switch	-	S-bus mode
S2	switch	-	Test signal

Application Information

Transformer Specifications

Table 8

S-Interface			
Parameter	**Min**	**Max**	**Units**
Turns Ratio	2 : 1		Line : Chip
Primary Inductance	20		mH
Leakage Inductance		13	µH
Interwinding Capacitance		50	pF nominal
PRI DCR	0.9	1.3	Ω (1.1Ω ± 20%)
SEC DCR	2.1	3.1	Ω (2.6Ω ± 20%)
U-Interface			
Parameter	**Min**	**Max**	**Units**
Turns Ratio	2 : 1		Line : Chip
Primary Inductance	13.5	16.5	mH
Leakage Inductance		60	µH
Interwinding Capacitance		90	pF
PRI DCR	6	7	Ω
SEC DCR	2.8	3.3	Ω

Master Clock and XTAL Connections

At the pins XTAL1 and XTAL2 a crystal must be connected to form a parallel mode oscillator. Two capacitors of 22 pF should be connected to ground.
Some crystals may require the parallel capacitor Cp to be used (10 pf Typ).

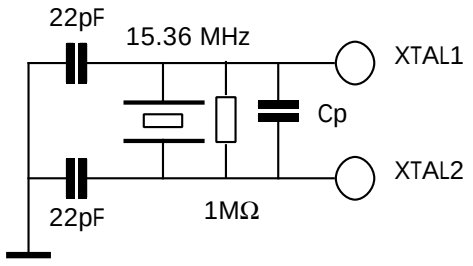


Fig.5: Crystal Configuration

Example Crystal Specifications

Table 9

AT cut, fundamental mode		
Parallel resonance frequency	15.360	MHz
Initial tolerance	± 50	ppm
Frequency drift	± 10	ppm
Dynamic capacitance	15	fF (info)
Load capacitance	30	pF
Parallel capacitance	7	pF (info)
Series resistance	40	Ω
Series resistance drift (age)	± 10	%
Drive level	0.25	mW

Overvoltage Protection

This is strongly dependant on the Printed Circuit Board layout and local specification variations. Generally, it is recommended to use standard small-signal diodes (e.g. 1N4004) to clamp voltages from the S- and U-interfaces to Vdd and ground. The recommended protection for the U-interface is to diode clamp the chip side transformer pins to the supply rails, and for the S-interface clamp the INTQ device pins (30, 31, 32, 33). In order to prevent excessive disturbance voltages from causing the power-supply voltage to increase (full-wave rectifier effect through the protection diodes), it is recommended that a zener-diode is used to clamp the Vdd voltage < 4,8V.

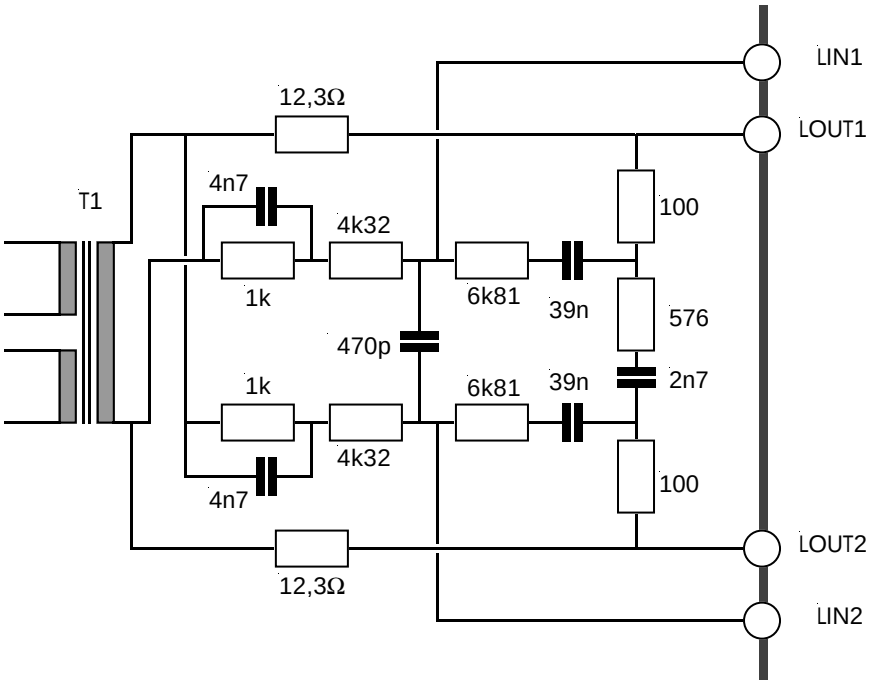
Unused Pins

The INTQ has a number of device pins which are used only in specific applications, or for device testing. These pins should be connected as shown below to ensure proper operation in a given application. '0' means connect to ground, '1' means connect to Vdd, 'open' means make no connection. A dash ('-') means that the pin is used in the application. All other pins have defined states as shown in the application schematic.

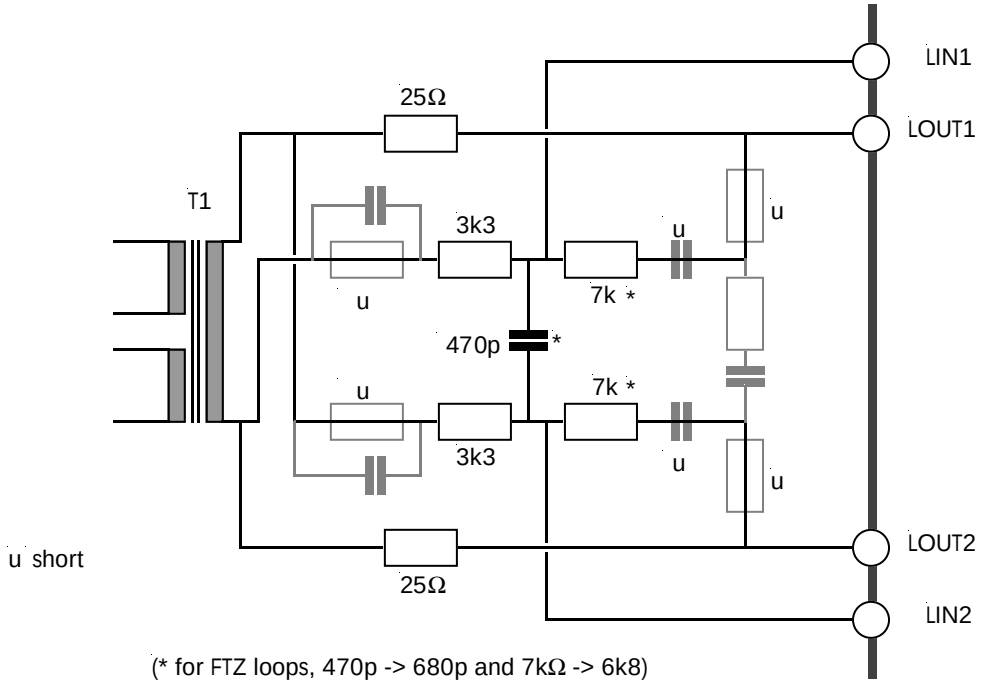
Table 10

Pin	Number	NT mode	NT+ mode
GMODE	22	0	1
G2DOUT	18	open	-
G2DIN	19	1	-
G2DCLK	20	0	-
G2DFR	21	0	-
G1DOUT	12	open / monitor	-
G1DIN	13	open / monitor	-
G1DCLK	14	open / monitor	-
G1DFR	15	open / monitor	-
TRST	5	0 (pull down)	0 (pull down)
TCK	6	1 (pull up)	1 (pull up)
TMS	7	1 (pull up)	1 (pull up)
TDI	8	1 (pull up)	1 (pull up)
TDO	9	open	open
CSO	29	0 (normal) 1 (CSO)	0 (normal) 1 (CSO)
PW40	38	-	-
PW220	39	-	-
TEST0	10	open	open
TEST1	11	open	open
OPTO	27	-	-
LED	28	-	-
SATP	34	open	open
TSP	40	0 (normal) 1 (test pulses)	0 (normal) 1 (test pulses)

Common Hybrid Schematics for 4B3T (MTC-20277) and 2B1Q (MTC-20276)



MTC-20276 - Recommended Hybrid component Configuration



(* for FTZ loops, 470p -> 680p and 7kΩ -> 6k8)

Fig .5a : MTC-20277 - Recommended Hybrid Component Configuration, using same PCB layout as 20276, (ETSI loops)

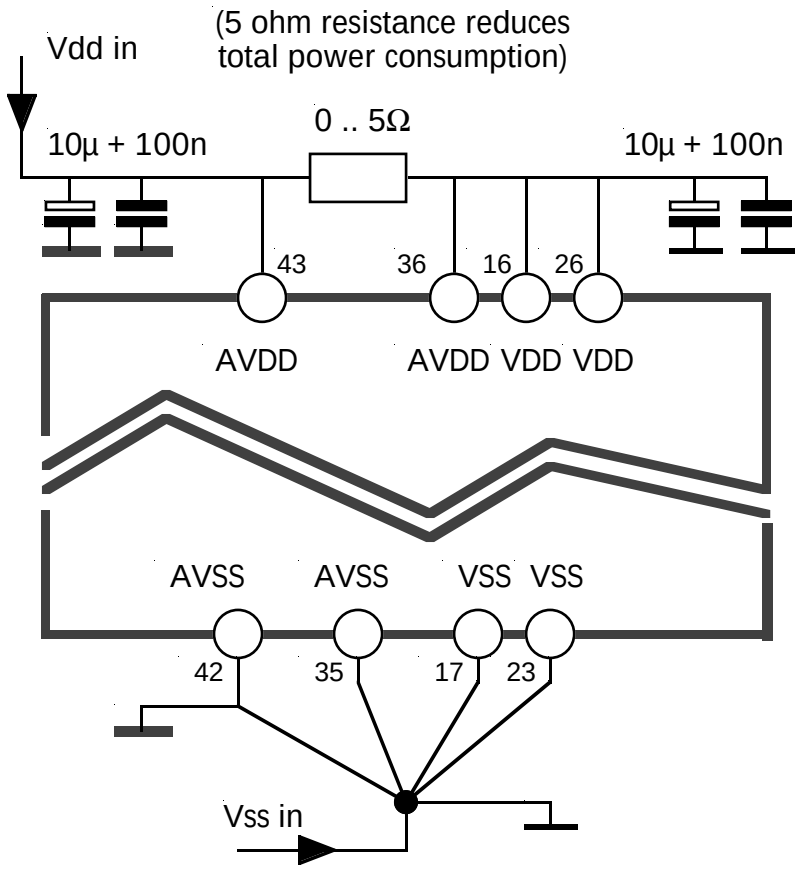


Fig. 5b : MTC-20276 / 20277 Recommended Power Supply Arrangement

Detailed Functional Description

U-Interface Block

Physical Characteristics

The quaternary symbol stream on the U-interface has to the following physical characteristics :

Symbol rate

The symbol rate is 80 kbaud ± 1 ppm and applies to synchronous symbol transmission.

Input Jitter

The INTQ tolerates a sinusoidal input jitter of the quaternary symbols as indicated in Figure 6.

Jitter Transfer Function

The jitter transfer function of the INTQ (looped between U-interfaces) doesn't exceed ± 1 dB in the frequency range 3 Hz to 30 Hz.

Output Jitter

The peak-to-peak jitter produced by the INTQ doesn't exceed 0.02 UI (≤ 166 ns), when measured via a high pass filter with a cut-off frequency of 30 Hz. Without this filter the same measurement doesn't read more than 0.1 UI.

Transmit Signal Amplitude

The absolute peak value VImax of a single pulse VI at the U0 interface terminated with a 135 Ohm resistance is 2.5 V ± 5%.

The absolute peak value of the coded quaternary signal measured at U0 interface terminated with 135 Ohm doesn't exceed 4 V.

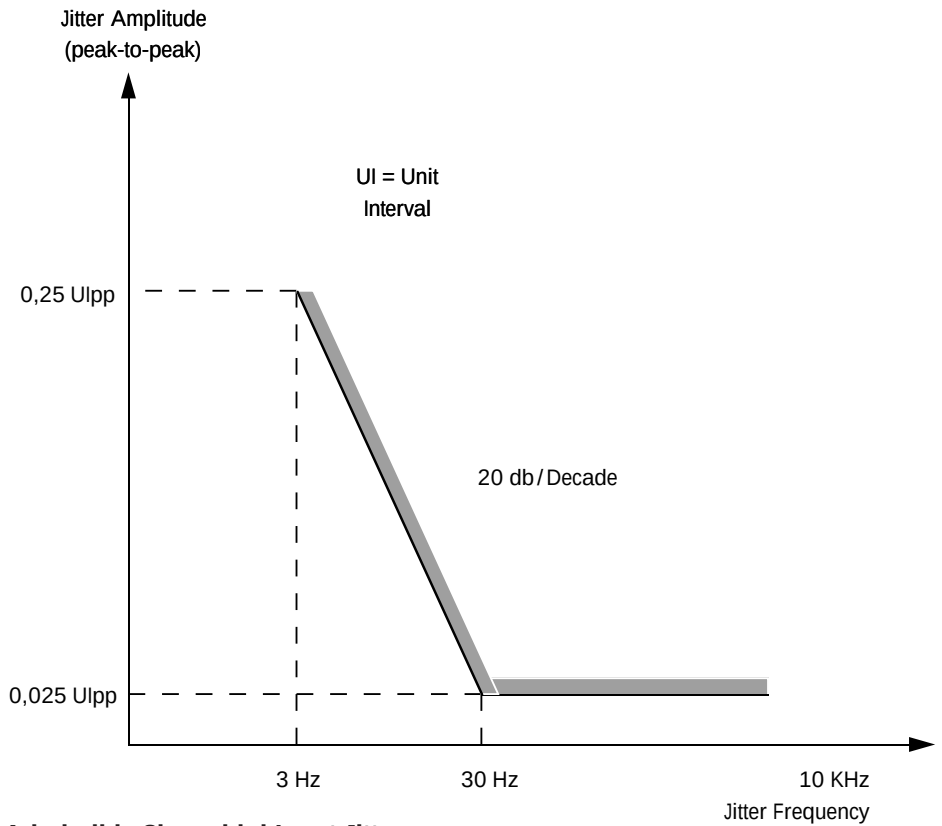


Fig.6: Range of Admissible Sinusoidal Input Jitter

Stability
The transmit signal amplitude measured over a period of one minute doesn't vary by more than 1% beginning 5 ms after the INTQ is switched into power-up state.

Transmit Spectrum
The spectrum of the quaternary transmit signal at U0 interface doesn't exceed the limits given in Figure 8.

Pulse Shape
A single pulse measured across a 135 Ohm resistance at U0 interface comply to the spectral requirements presented in Figure 8 and the pulse mask requirements given in Figure 9.

Maximum Voltage
The maximum peak-to-peak value VUmax of the voltage VU as shown in figure 7 with full receive signal (short line), that can be accepted is 2 V. Due to the analog echo subtraction the maximum peak-to peak value Vinmax of the voltage Vin between LIN1 and LIN2 is 1.35 V.

Input/Output Impedance
The line terminating impedance is nominally 135 Ohm in power up and power down states. The return loss against 135Ω real exceeds 16 dB between 12 kHz and 50 kHz.
- slope below 12 kHz : 20 dB / decade
- slope above 50 kHz : -10 dB / decade

Load
The load is given by the line transformer and the subscriber line. The loops are standardised by the ANSI and ETSI documents.
- Turns ratio of line transformer : 2:1
- Transformer coil inductance (from line side) : 15 mH ± 10%

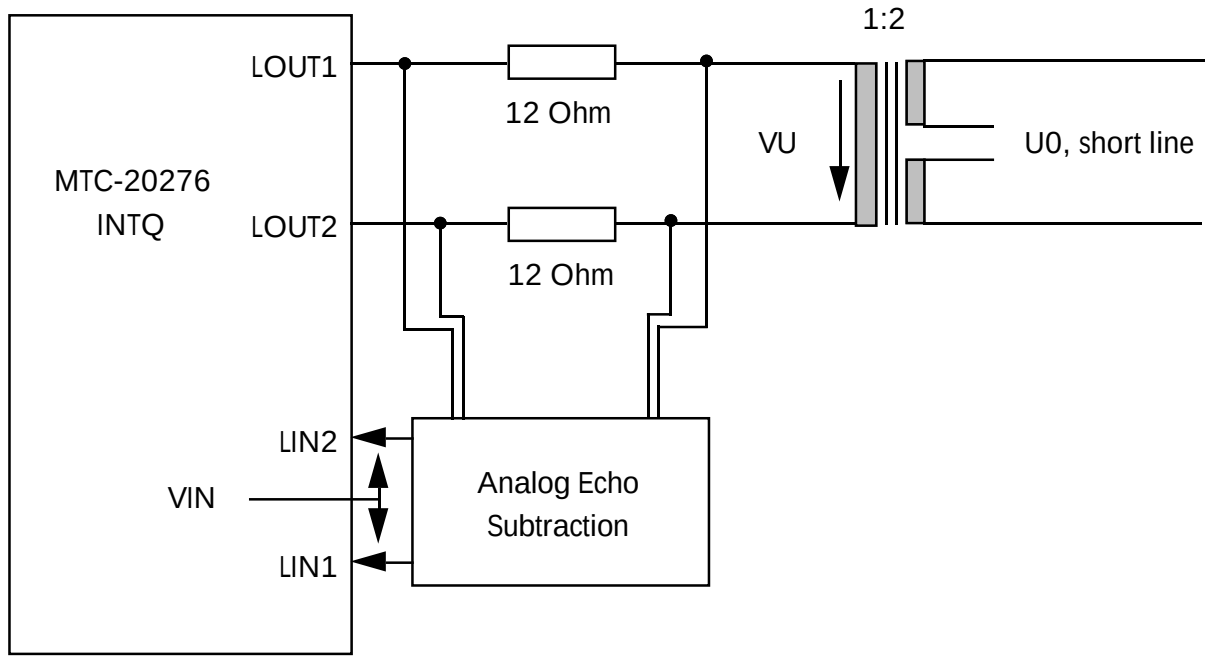


Fig.7: Test Circuit for Voltages VU and VIN, U0 Interface

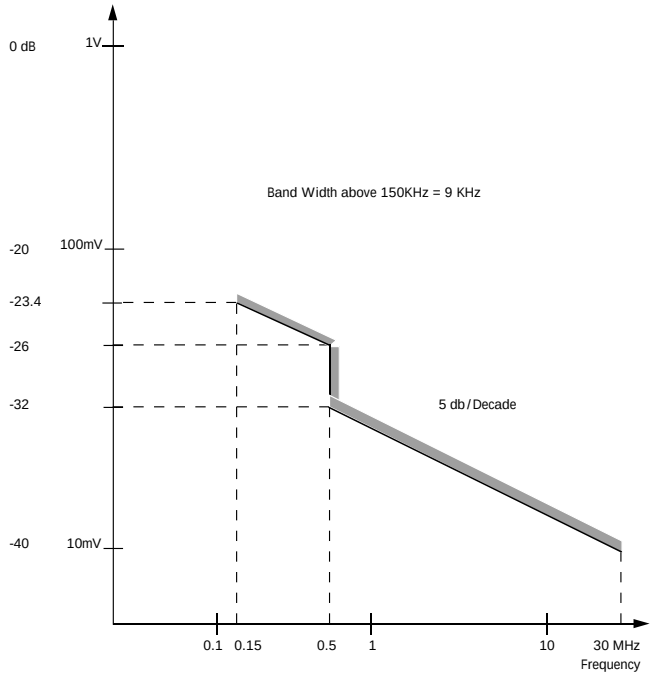


Fig.8: Spectrum of Signal at U0 Interface

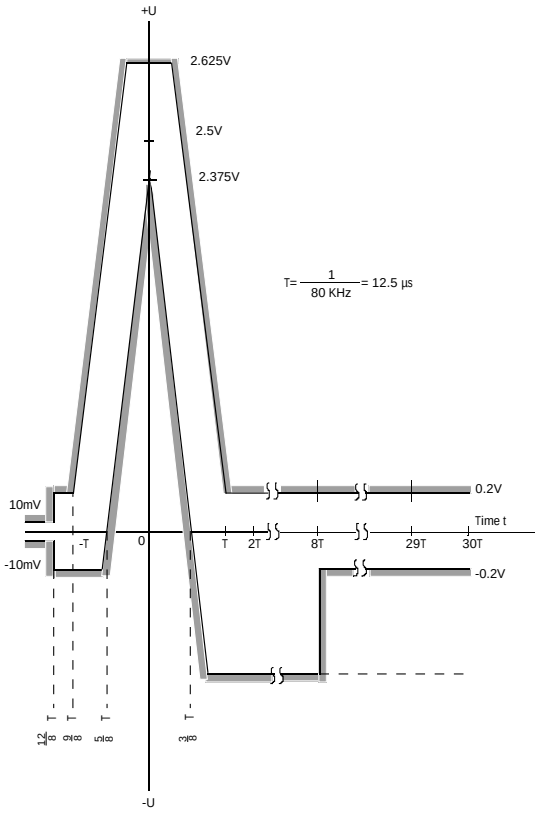


Fig.9: Single Pulse Mask

Logical Characteristics of the U-Interface

The quaternary symbol stream crossing the U-interface complies with the following logical characteristics :

Frame Structure

The information flow across the subscriber line uses frames as shown in Figure 10. The length of such a frame corresponds to 120 quaternary symbols being transmitted within 1.5 ms. The frame structure is detailed as follows:

B+B+D - Data

108 quaternary symbols represent 216 bits of scrambled and encoded B+B+D data. The 108 quaternary symbols are transmitted in succession. These blocks are assembled as follows:

Data of					
B1 + B2 + D	+ B1 +	B2 +	D		
Number of bits					
8	8	2	8	8	2

Synchronising Word

9 quaternary symbols in each direction represent a non-scrambled synchronising word. They are used to generate frame clocks. If they are out of position for 60 ... 200 consecutive frames, the line resynchronization procedure is started. The quaternary values and the frame position are as follows:

1. From LT to NT or analog loop in LT (loop 1) or analog loop on NT, and from NT to LT.

SW Polarity :	+3	+3	-3	-3	-3	+3	-3	+3	+3
ISW Polarity :	-3	-3	+3	+3	+3	-3	+3	-3	-3

Quad Position	1-9	10-117	118-120
Bit Position	1-18	19-234	235-240

Frame 1	ISW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6
Frame 2	SW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6
Frame 3	SW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6
Frame 4	SW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6
Frame 5	SW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6
Frame 6	SW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6
Frame 7	SW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6
Frame 8	SW	2B+D	2B+D	...	2B+D	2B+D	M1	...	M6

SW-Sync Word
ISW-Inverted SW

M1-M6
Mantenance Channel

Fig.10: Frame and Superframe Structure

Maintenance and Service Channel

3 quaternary symbols per frame are transmitted to convey maintenance and embedded operations channel information. This information is contained in a superframe consisting of 8 frames (duration: 12 ms). The start of a superframe in up and downstream directions is market by a single inversion of the synchronisation word (ISW). The quaternary symbol sequences represent data that can be transmitted at a rate of 4 kbits/s. They are transmitted immediately before the sync word (SW).

The M symbol is used for various purposes incluiding:

1. Maintenance Channel (control test loops and report frame errors)
2. Service channel (carry transparent user data in both directions)

In detail the following convention applies (NT to LT):

Table 11

	M1	M2	M3	M4	M5	M6
Frame1	EOC a1	EOC a2	EOC a3	ACT	1	1
Frame 2	EOC dm	EOC i1	EOC i2	PS1	1	FEBE
Frame 3	EOC i3	EOC i4	EOC i5	PS2	CRC 1	CRC 2
Frame 4	EOC i6	EOC i7	EOC i8	NTM	CRC 3	CRC4
Frame 5	EOC a1	EOC a2	EOC a3	CSO	CRC 5	CRC6
Frame 6	EOC dm	EOC i1	EOC i2	1	CRC 7	CRC8
Frame 7	EOC i3	EOC i4	EOC i5	SAI	CRC9	CRC10
Frame 8	EOC i6	EOC i7	EOC i8	1	CRC 11	CRC 12

Service and Maintenance Data Convention

Table 12

Symbol	Description
ACT	Activation bit (set to ONE during activation)
CRC	Cyclic Redundancy check: covers 2B+D & M4: 1= most significant bit; 2= next most significant bit, etc.
CSO	Cold-start-only bit (ONE indicates cold-start-only)

EOC	Embedded operations channel:
	a = address bit;
	dm = data/message indicator;
	i = information (data/message).

FEBE	Far end block error bit (ZERO for errored multiframe).
NTM	NT in test mode bit (ZERO indicates test mode).
PS1/PS2	Power status bits (ZERO indicates power problems).
SAI	S-activation indicator bit (optional, set = 1 to activate S/T

Note: Transmission errors in the data protected by the Cyclic Redundancy Check are detected during each superframe and reported back to the LT in the next superframe. This is for loop quality checking only and does not invoke retransmission of any sort.

Encoding

The encoding of a binary bit stream is such that 2 binary bits correspond to 1 quaternary symbol. The first symbol of a frame will always contain the information of the first 2 bits of a B1 channel (although these bits are of course scrambled).

In the receive direction, the first symbol of the quaternary frame is always converted (after descrambling) into the first two bits of a B1 channel.
The exact convertion is done according to the following rules (ANSI specification):

Table 13

Quaternal Symbol	First bit (Sign)	Second Bit (Magnitude)
+3	1	0
+1	1	1
-1	0	1
-3	0	0

Scrambling

The received binary data stream is divided by generating polynomials.

The scrambler contains supervision circuitry which flags if a continuous series of ones or zeros have been detected at the output for a complete 1 ms frame.

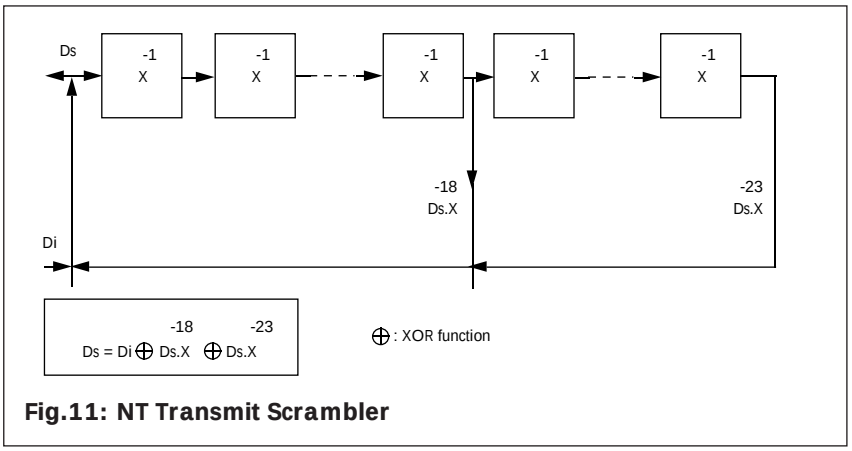


Fig.11: NT Transmit Scrambler

Descrambling

The quaternary signals received on each side of the subscriber line are converted back into a binary bit stream and multiplied by the generating polynomials in order to recover the original data.

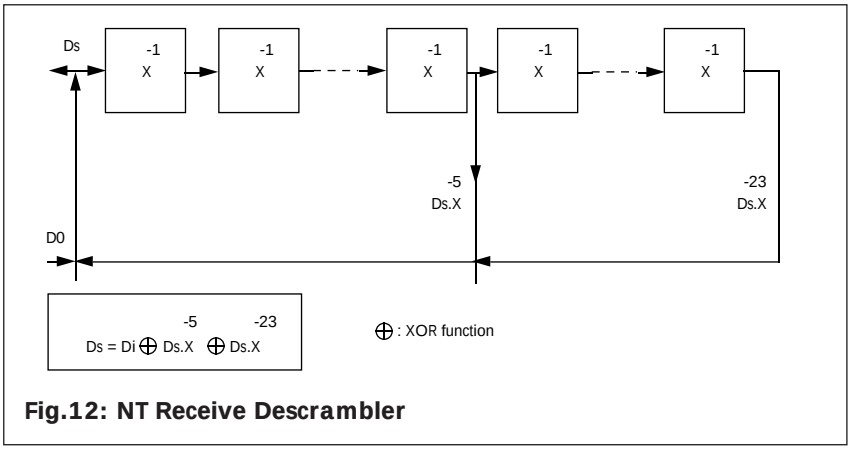


Fig.12: NT Receive Descrambler

Activation and Deactivation

In order to reduce the power consumption of circuits connected to the subscriber line, INTQ can be switched to stand-by or powered down during idle periods. The components are powered up again during the line activation procedure. Two states are defined :

- Power-down state
Power consumption of the majority of the functions is reduced by stopping the clocks; maximum power reduction;

- Power-up state
All functions powered up; GCI interface is activated; exchange of C/I messages is possible.

The activation procedure consists of three phases : awake (see the following sections), synchronise, and connect through.

Maximum activation time (from command ACT to indication CT) without repeater :
≤ 170 ms under normal conditions (starting with stored coefficients)
1 s after reset of the coefficients.

The deactivation procedure consists of two phases : line deactivation of the NT can be initiated only by INFO U0.

Deactivation time (from Command DEAC to Indication DC) is in the order of 4 ms.

Reset

The INTQ can be reset via an external pin (NRESET = LOW) or via the command RES in the C/I channel. Normally the INTQ is reset via the pin NRESET (hardware reset).

Both reset requests cause a reset for various function blocks via the activation/deactivation control and the reset logic. The INTQ is initialised such that a “cold start” (resetting of the coefficients) is possible.

Analog Loop (Loop 2 in NT)

For maintenance purposes a loop can be closed by applying the correct command into the M channel or into the GCI C/I channel, described in the next section.

GCI Interface, Common Functions

Data Format and Timing of the GCI Interface (DIN, DOUT, DCLK, DFR)

Continuous Modes

Nominal bitrate of data (DIN and DOUT)	256 kbit/s
Nominal frequency of clock (DCLK)	512 kHz
Peak-to-peak output jitter (DCLK)	≤ 166 ns
Nominal frequency of frame clock (DFR)	8 kHz
Mark-to-space ratio of DFR, i (input)	1:2 . . . 2:1
Mark-to-space ratio of DFR, o (output)	0.4:0.6 . . . 0.6:0.4

Figure 13 shows the timing of data and clocks at the digital interface 256 kbit/s (continuous modes).
Transitions of the data occur after even numbered rising edges of the DCLK. The data is valid on the odd numbered rising edges of the DCLK. Even-numbered rising edges of the clock are defined as the second rising edge following the rising edge of the frame clock and every second rising edge thereafter.The maximum allowed jitter is shown in figure 14.

The start of the frame is marked by the rising edge of the frame clock DFR.

One frame contains four time slots. The data streams at DIN and DOUT consist of four bytes per frame. See figure 15. The input data DIN and the output data DOUT are synchronous and in phase.

In the power-down state, the signal at DIN and at DOUT is high and the signal at DFR and DCLK is low.

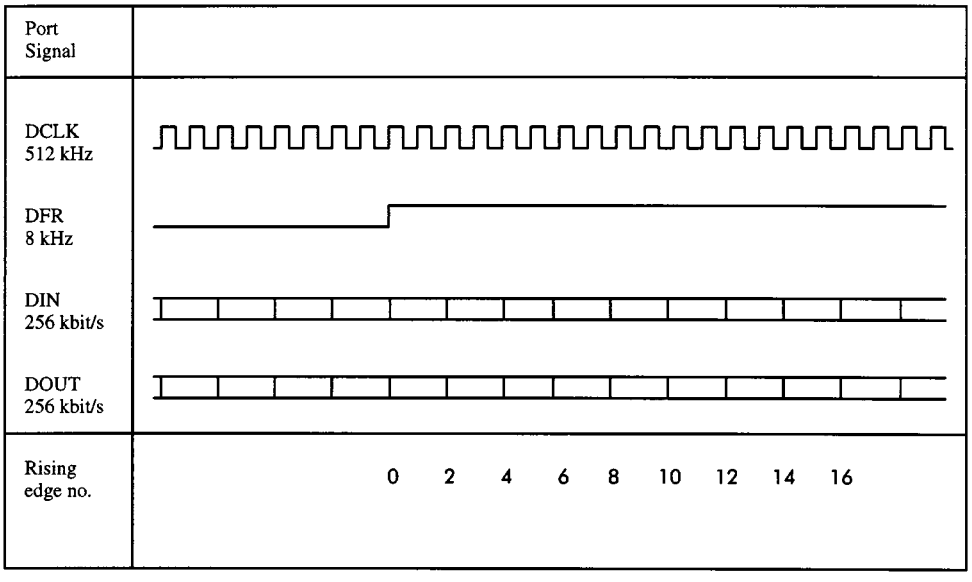


Fig.13: Timing of Data and Clocks at the GCI Interface

The GCI Interface

At the digital control interface the S-interface block is connected via a bidirectional serial interface, a digital bus called the General Circuit Interface (GCI), also called the ISDN Oriented Modular (IOM) interface. This bus is logically organized as many parallel point to point links, each at 256 kbit/s. The description of the GCI is available in the related documents and on page 23.

The Physical Organization of the GCI Bus

The bus has a clock and frame signal as timing, and two data lines, one for each direction.
In NT mode the S-interface receives the GCI timing.

General Content of the GCI Bus

The GCI interface is organized with 4 channels at 64 kbit/s: B1, B2, M (Maintenance or Monitor), and B1* channel.
The B1 and B2 channels are transparent, switched at 64 kbit/s.

In ISDN applications the B1* channel contains two D-channel bits, 4 bits C/I channel with the commands (towards S-interface) or the indications (from S-interface), and two extra bits (MR and MX) to control the M-channel.

The D-channel contains HDLC messages. It is transported transparently (NT) or terminated by an HDLC transceiver (LT-S/LT-T/TE). In the TE/LT-T a D-channel access protocol exists on the S-bus, which must be controlled by the S-interface, and obeyed by the HDLC transmitter.
-
Via the Command/Indication (C/I) channel, Commands to, and state Indications from the S-interface are exchanged with a control element (microcontroller) or with another uplink or downlink ISDN circuit. Commands and Indications are debounced to avoid erroneous behaviour.

The M-channel is a 64 kbit/s channel. It has a byte oriented structure, and the content is indicated and acknowledged with the MR and MX bits, the two last bits in the B1* channel. Content of the channel: write and read access of internal S-interface registers.

Power-down on GCI

For maximal power saving the GCI bus can be halted completely, and reactivated asynchronously from either side of the bus.

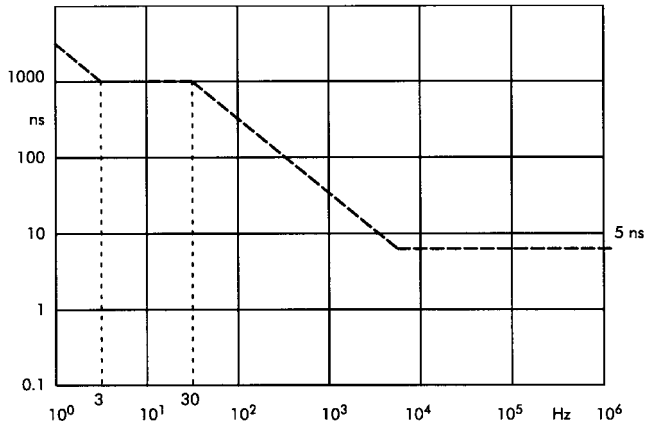


Fig.14: Maximum Admissable Peak-To-Peak Input Jitter of Clocks (DCLK, DFR) at the GCI

Frame Format

4 bytes are transmitted in each frame:

1st byte B1:
B-channel (64 kbit/s data), transparent

2nd byte B2:
B-channel (64 kbit/s data), transparent

3rd byte B2*:
Monitor channel, DIN: 8 bit address, MSB first, DOUT: 8 bit data

4th byte B1*:
2 bit D-channel (16 kbit/s data)
4 bit C/I channel A1, A2, A3, A4
A, E bit used to control the transfer of information on the Monitor channel

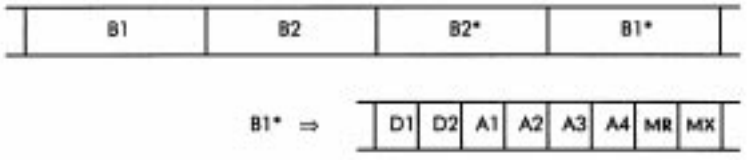


Fig.15: GCI Frame Format

External GCI Interfaces

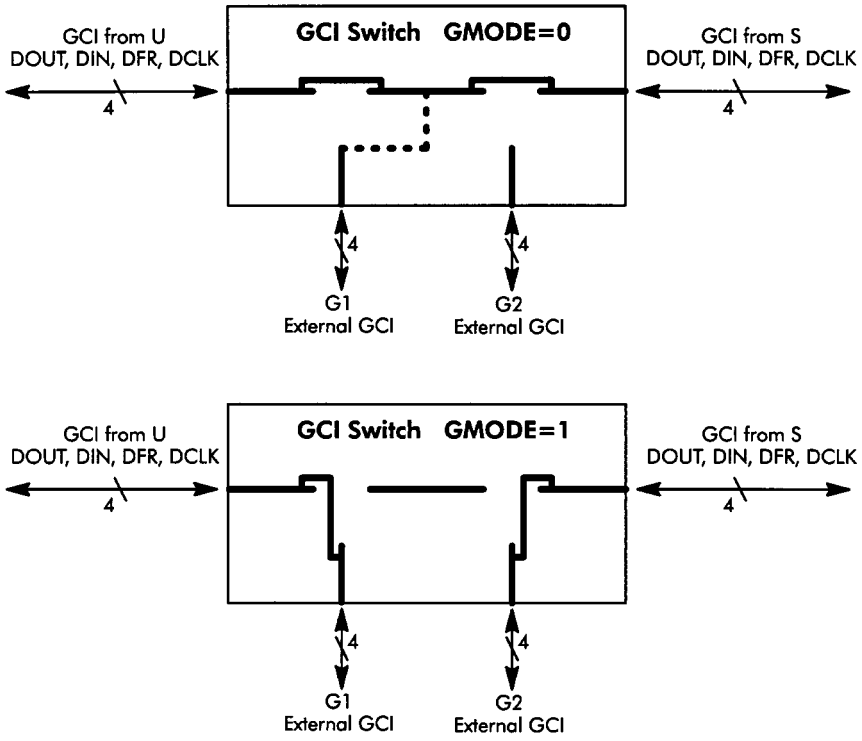


Fig. 16: External GCI Interface

G1 External GCI Interface

Figure 16 shows a schematic representation of the two possible modes of the GCI ports.
In normal mode, corresponding to pin GMODE low, the two internal GCI interfaces are connected. The G1 interface is used as a monitorpoint.

In NTplus mode, corresponding to pin GMODE being high, the GCI interface coming from the U-interface block is connected to the G1 External GCI.

The S-interface block is connected to the G2 External GCI.

The U-interface block is the master of the GCI interface and thus controls the GCI clock (DCLK) and the GCI frame (DFR). DCLK and DFR signals at the G1 interface are outputs of the INTQ.

G1 interface characteristics:
- G1 DOUT: output, data channel, 256 KHz
- G1 DIN: input in NTplus mode, output in normal mode; data channel, 256 KHz
- G1 DFR: output, frame clock, 8 KHz
- G1 DCLK:output,clock, 512 KHz

G2 External GCI Interface

In normal mode, corresponding to pin GMODE low, the two internal GCI interfaces are connected together. G2 interface has no function.

In NTplus mode, corresponding to pin GMODE high, the GCI interface of the S-interface block is connected to the G2 External GCI.

The S-interface block is the slave of the GCI interface, so the GCI clock (DCLK) and the GCI frame (DFR) signals at the G2 interface are inputs of the INTQ .

G2 interface characteristics:
- G2 DOUT,: output, data channel, 256 KHz
- G2 DIN,: input, data channel, 256 KHz
- G2 DFR: input, frame clock, 8 KHz
- G2 DCLK: input, clock, 512 KHz

U-Interface Command List

The evaluation of any command is done according to a double last look criterion: any command is recognized only after the same command has been detected in two successive frames. Until then the preceding command is considered valid.

If commands are received that are not included in the list, the last recognized command is considered valid. Commands which are logically impossible to receive in the current state are ignored (ref. ETR 80).

The indications are transmitted continuously in each frame. Under no circumstances can an indication that is not included in the list be transmitted.
The maintenance and Service Channel, and the B2* Channel are not used by the U-interface block.

Command and Indicate (C/I) Channel (A bits)

Command (DIN) (from GCI to U).

Table 14

Awake	0000: AW	This command is to be used when the deactivated module interface is to be set in the power-up state. The control may be represented by a steady-state binary '0' condition at DIN. The module interface will be activated, i.e. provided with bit and frame clocks for synchronous transmission. Any other command may now be applied. The command AW, however, maintains the activated state of the module interface without emission of any signal at U0.
Activate	1000: ACT	Layer 1 is activated at the U0 interface, starting with transmission of the wake-up signal INFO U1W. After execution of the wakeup procedure, the transmitter generates INFO U1A during synchronization process. When synchronization is completed successfully, the transmitter outputs INFO U1.
Synchronized	1100: SY	When the synchronization process of the receiver is completed successfully, the transmitter outputs INFO U3. After reception of INFO U4H, Connect Through (CT) is indicated and the INTQ will be connected through from module interface to line interface (transparent).
Deactivate Confirmation	1111: DC	This control has to be used if the reciever is to be able to recognize awake-signals at interface U0, but the transmitter still is disabled. If no wake-up signal is recognized, the INTQ is set to its power-down state. The module interface will be deactivated.

Indication (DOUT) (From U to GCI)

Deactivate	0000: DEAC	A request to deactivate level 1 (INFO U0) has been detected. INFO U0 is transmitted at U0.
Test mode 1	0010: TM1	Forces S-interface in test mode 1, sending single zeros. Not supported by the U-interface but recognized by the S-interface (NT mode only)
Resynchro-nization	0100: RESYN	The receiver has lost framing and is attempting to resynchronize. The INTQ remains connected through from module interface to line interface (transparent).
Activate	1000: ACT	The synchronous state of the receiver is established (without a loop 2 or a loop 4 command). The transmitter outputs INFO U1.
Loop 2	1010: L2	The synchronous state of the receiver is established with a loop 2 command. The transmitter outputs INFO U3.
Connection Through	1100: CT	INFO U4H has been detected at the U-interface. The INTQ will be connected through from module interface to line interface (transparent).
Connection Through with Loop 2	1110: CTL2	INFO U4H and a loop 2 command have been detected at the U-interface. The INTQ will be connected through from module interface to line interface (transparent).
Deactivated Confirmation	1111: DC	The transmitter is disabled, but the receiver remains enabled to detect wake-up signals at the U-interface. The INTQ is set in its power-down state, as long as wake-up signals are not recognized. When a wake-up procedure is finished, INFO U1A is transmitted.

Power Down of the Interfaces

In the following description, the U-interface port of the GCI interface (G1) is the master, and the S port of the GCI (G2) is the slave.

Transition from Synchronous to Power-Down State

The corresponding procedure is shown in figure 17. After a DC code has been detected at the module interface of the master in two successive frames from the slave, the master responds by indicating DC four times and then the master turns off the timing signals at the end of bit A4 of the fourth DC indication. After this time, the DOUT pins of master and slave must be kept HIGH (quiescent condition).

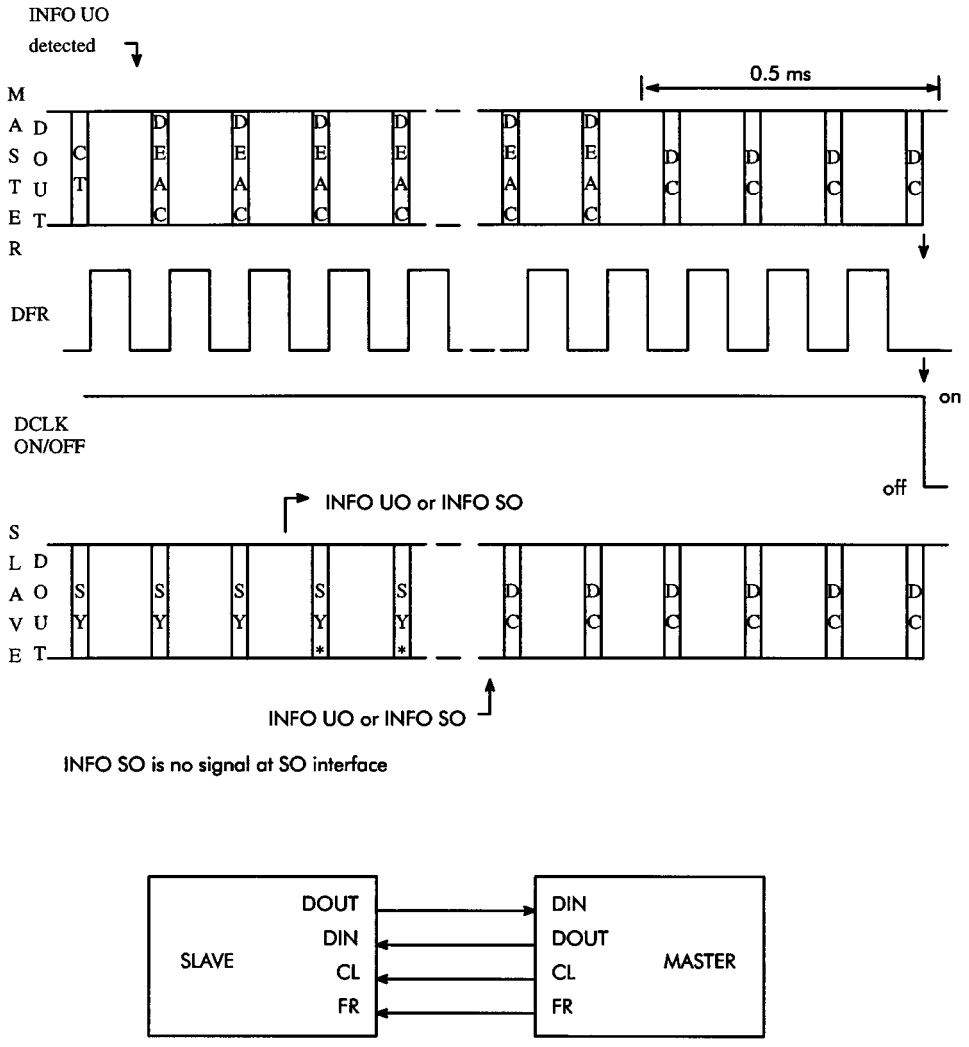


Fig.17 Transition to Power-Down State

Wake-up Originated by Slave

Transition from power-down to synchronous operation is initiated by the slave by transmitting LOW at DOUT. See the figure above.
The master responds by turning timing signals on within the wake-up time Taw (typical 4 ms, max. 10 ms). To ensure continuous supply of timing signals by the master the slave must keep DOUT LOW.

After the timing signals have been detected by the slave, the slave must transmit AW for at least two frames (e.g. 8 frames). Then the slave may insert a valid code in the C/I channel (e.g. ACT).
Monitoring of pin DOUT for LOW by the master will start only after the timing signals have been turned off.

It is required that the clock signals at DCLK and DFR will have the nominal frequency with the specified tolerance from the moment they are turned on. The slave may deactivate the master if only AW (not yet ACT) has been detected by the DC command or by transmitting continuous HIGH at DOUT. The master will respond by turning off the timing signals. See figure 18.

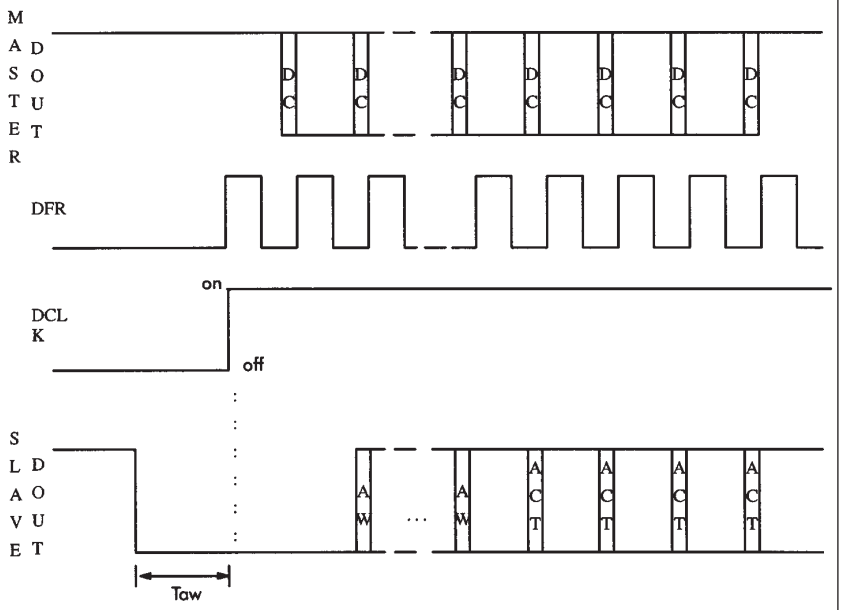


Fig.18: Wake-up Initialisation Procedure, upstream

Wake-up Originated by the Master

Transition of the device from power-down to synchronous state can be initiated by the master by turning on clock signals DCLK and DFR. Simultaneously, the master must apply the desired command code in the C/I channel.

The slave may enter the power-up state immediately after clock signals have been applied, and the received command code has been evaluated. See figure 19.

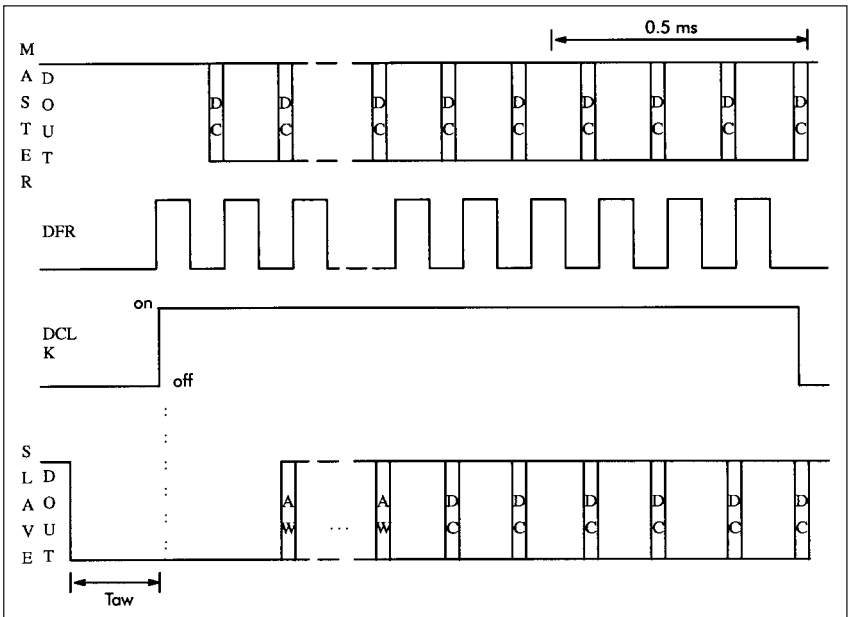


Fig.19: Wake-up Initialisation Procedure, downstream

S-Interface Commands and Indications Summary.

Table 15

NT	Downstr Command	Upstr. Indicat.		Downstr Command	Upstr. Indicat
0000	DR	TIM	1000	ARd	ARu
0001	RES	(lsl)	1001	-	-
0010	ssz=TM1	-	1010	ARL	-
0011	TM2	-	1001	-	-
0100	RSYd	RSYu	1100	AId	AIu
0101	-	-	1101	-	-
0110	-	ei	1110	AIL	-
0111	-	-	1111	did=DC	DIu

Commands (Downstream) in NT Mode

Table 16

0000	DR	Deactivate Request	Forces the S-interface block to deactivate the S-bus (=INFO0) followed by DIu and did=DC
0001	RES	RESET	Forces S-interface to soft reset, extended mode only, S-interface accepts it in basic mode (merged)
0010	ssz = TM1	TEST-MODE 1	Forces S-interface to test-mode 1, sending single zeros
0011	TM2	TEST-MODE 2	Forces S-interface to test-mode 2, extended mode only, sending continuous zeros.
0100	RSYd	Resynchon-izing down	The U-interface is not synchronous, S-interface sends INFO2 {or SCZ}, see remark 1 below
1000	ARd	Activation Request down	MTC-20172 S-interface forced to INFO2 transmission, receiver indicates the S-bus reaction
1010	ARL	Activat. req with S-loop	INFO2 transmission on the S-bus test loop2 switched (transparent loop)
1100	AId	Activation Indication	INFO4 transmission, normally only after AIu indication is received
1110	AIL	Activ. Indic. with S-loop	INFO4 transmission test loop2 switched (transparent loop)
1111	did= DC	Deactivate Confirmation	Deactivation confirmation, entering the power down state, INFO0 sent, critical timing to halt the clocks.

Remark 1: When the U-interface is resynchronizing, the S-interface will send INFO2.

Remark 2: During loops, the S-interface simply ignores the incoming INFO3 from the S-bus. The receiver synchronizes on looped INFO2/4.

Indications (Upstream) in NT Mode

Table 17

0000	TIM	Timing Request	The S-interface requires GCI clocks.
0100	RSYu	Resynchron-izing	The S-bus receiver tries to synchronize
0101	---------	---------	---------
0110	ei	Error Indication	RSTB and SCZ- pin both low simultaneously
1000	ARu	Activation Request up	INFO1 received (actually any AMI signal)
1100	Alu	Activation Indication up	Receiver synchronized on INFO2/3/4 (INFO3 normally, INFO2/4 in loop)
1111	Dlu	Deactivation Indication	Timer (32 ms) expired, or INFO0 received (16 ms) after DR (deactiv. request)

The S-Interface

Functional Overview

For transmission of data over the subscriber premises, the S-interface provides the S_0-interface. This interface enables full duplex transmission of data (2B + 1 D-channel) over 4 wires at a nominal data rate of 192 kBits/s. An Alternating Mark Invert (AMI) code is used for the line transmission. The transmission of data over the S_0-interface consists of frames of 250 µs. Each frame is 48 bits wide, and contains 4 data bytes (2 B1, 2 B2) and 4 D-bits.

The frame structures are shown in fig.20.
A frame start is marked using a first code violation (no mark inversion).
To allow secure synchronization of the receiver, a second code violation is generated before the 14th bit of the frame. To guarantee this second violation, an auxiliary framing bit pair FA and N (from NT to TE) or the framing bit FA with associated balance bit (from TE to NT) are introduced.

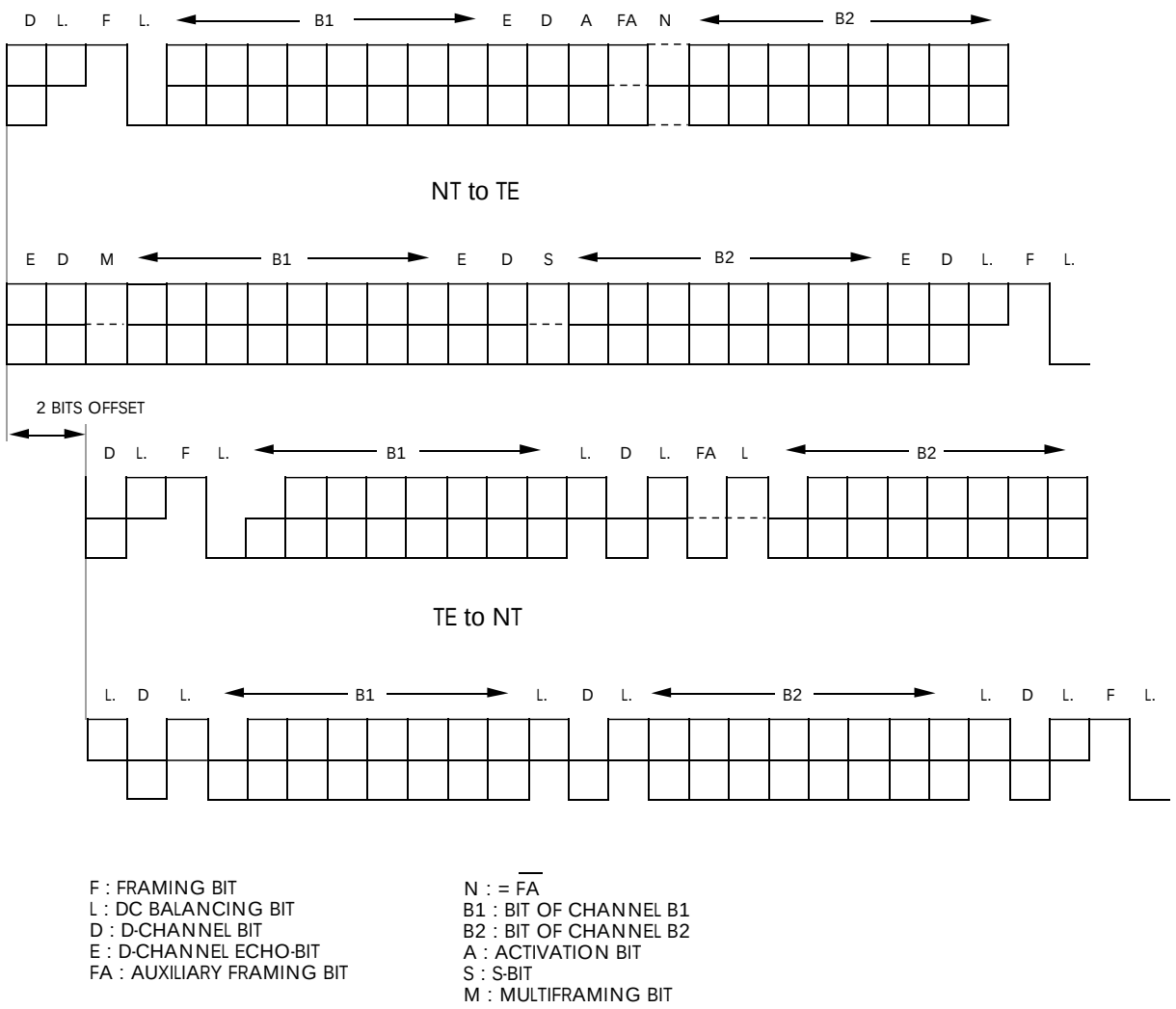
The first bit of the transmitted frame from TE to NT is delayed for 2 bit periods with respect to the frame received from the NT. Furthermore, an echo bit (E-bit) for the D-channel and an activation bit (A-bit) are provided, where DC-balancing is done by means of the L-bits.

General Description of the S-bus Interface

The S-interface can be used on the S-bus configured as a point-to-point connection or as a passive bus. The bus connection can handle up to 8 terminals. It is either a short bus with the terminals dispersed over a length of 200m, or an extended bus with a cluster of terminals within a 25 m range.
The chip handles full-duplex transmission of two B-channels (64 kbit/s each) and one D-channel (16 kbit/s). It handles also the echo E-channel, the multiframing S and Q bits, ...
The S-interface contains all circuit parts necessary for the adaption of the S-interface, especially transmitter and receiver stages.

- S-bus outputs are balanced, allow ing bus operation;
- S-bus inputs are balanced;
- Out-of-band noise is filtered;
- RX has AGC and an adaptive threshold, and corrects long-line distortion by optimizing the sample moment.
- NT receiver bus type is selectable: short bus with fixed timing, or adaptive timing for extended bus or point to point.

The S-bus tranceiver stages must be connected to the bus via external interface circuitry (2:1 transformer) and protection. When the S-interface is in unpowered state (supply voltage = 0 V) the S-bus transmitter is high ohmic (see CCITT I.430).



F : FRAMING BIT
L : DC BALANCING BIT
D : D-CHANNEL BIT
E : D-CHANNEL ECHO-BIT
FA : AUXILIARY FRAMING BIT

N : = $\overline{FA}$
B1 : BIT OF CHANNEL B1
B2 : BIT OF CHANNEL B2
A : ACTIVATION BIT
S : S-BIT
M : MULTIFRAMING BIT

Fig. 20 : So-Frame Format

The S -interface can be used in a point-to-point and in a point to multipoint configuration (including extended passive bus). In the first configuration, the length of the cable is limited to aprox. 1.2 km (see fig.21).

In the bus configuration (point to multipoint), up to 8 terminals may be connected to the S0-interface (fig.22) The terminals must be connected in a range of 150 m. For the extended passive bus, the terminals must be clustered within a 25m range with a maximum cable length of about 1 km.

To avoid bus mismatching when multiple TEs are connected, the driver stages present a high impedance when they are not powered.

Controlled access to the shared data channels is realized within the S-interface by a D-channel access procedure. Each terminal can be given a certain priority for D access. Via the echo bit, which is the reflection of the received D channel at the NT, it is possible for the terminal to detect the status of the D-channel. In order to try to gain access over the D-channel, a terminal has to see 8 to 11 consecutive ones in the echo-channel. The exact number depends on the priority given to the terminal. When several terminals try to gain access at the same time, collisions occur on the S-bus. The terminal that transmitted "one" but sees a “zero” in the echo channel detects the collision and loses the D-channel access.

The terminal that transmitted the "zero" gains the access. When a successful D-channel message is transmitted, the priority is decreased by 1 in order to guarantee fairness with the other terminals. The status of the D-channel of the TE/LTT is at the 5th bit position of the monitor byte. This enables the control of the D-channel by an external HDLC controller.

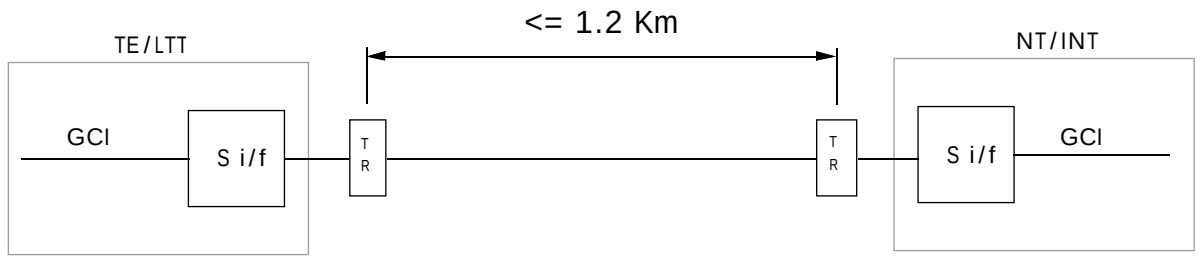


Fig. 21 : Point to Point Configuration

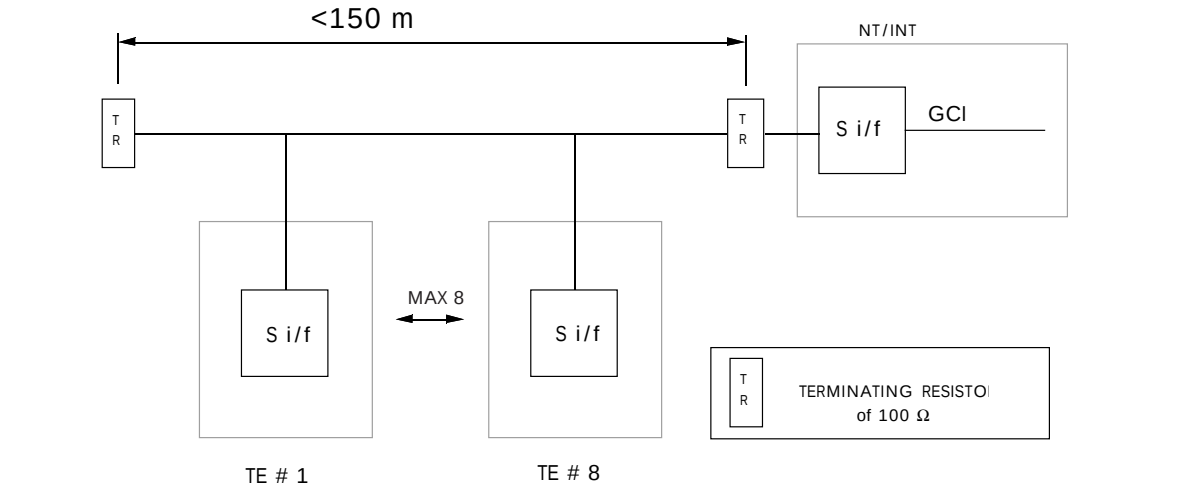


Fig. 22 : Point to Multipoint Configuration

S-Interface General Overview

The block diagram of the S-interface is shown in fig.23.

Data from the So-interface is received by the S-interface receiver, which has a balanced input, an AGC stage, a filter and comparators with dynamically adapted thresholds. The timing of the received S_0-frame is fixed (Only NT).

In the fixed timing case, the timing is locked to the transmitted frame, and the tolerable phase delay on the received So-frame is limited. In adaptive timing mode, delays up to 48 µs can be tolerated. The start of the received frame is detected in the FL-detection unit. An adaptive algorithm is used for compensation of the slope of the FL transition. A digital PLL recovers the received bit clock (192 kHz).

A second digital PLL generates the transmit bit clock (192 kHz), which is locked to the GCI frame. It is possible to compensate external circuits (e.g. filters) by adjusting the internal phase of the bit clocks by means of a register accessible by the monitor channel.

These circuits work with a 7680 kHz ±100 ppm clock. This clock is internally delivered to the S-interface by the U-interface block.

The serial B and D data from the V* GCI digital-interface is stored into a buffer with a dynamic pointer structure, and is presented to the S_transmitter where the So-frame formatting is done. In the other direction, the S_receiver unit disassembles the received So-frame.

The B and D data are stored in the buffer and multiplexed together with M, C/I, MX and MR into a digital V* GCI frame. The pointer structure of the buffer guarantees a minimum round-trip delay. If the clock wander becomes too big, a warning is given in the C/I channel, and the internal pointers are reinitialized.

Activation/deactivation procedures are handled in the status controller. Two basic modes are available: A V* mode, compatible with the U-interface block, and a GCI compatible mode. The S-interface automatically selects the connect mode.

The S/Q control module handles the multiframing on the S and the Q channel of the So-interface. This function is disabled in the INT.

In order to reduce the power consumption of the components connected to the subscriber line, the S-interface are switched to a power down mode during idle periods.

Test Modes Summary

Test loops may be closed in the S-interface, where all three channels (B1, B2 and D) are looped back as close as possible to the So-interface.

Loop 2 is a transparent loop where the transmitted So-frame is also switched on the S-bus. Activation from the So-interface is not possible.

Both loops are initiated over the C/I-channel and under control of a layer 2 component.

For further testing of the subscriber line, two test signals can be transmitted over the So-interface: A 96 kHz test sequence sending continuous AMI marks, and a 2 kHz test sequence sending single AMI marks. Both test modes are under control of the C/I channel, as well as TSP pin.

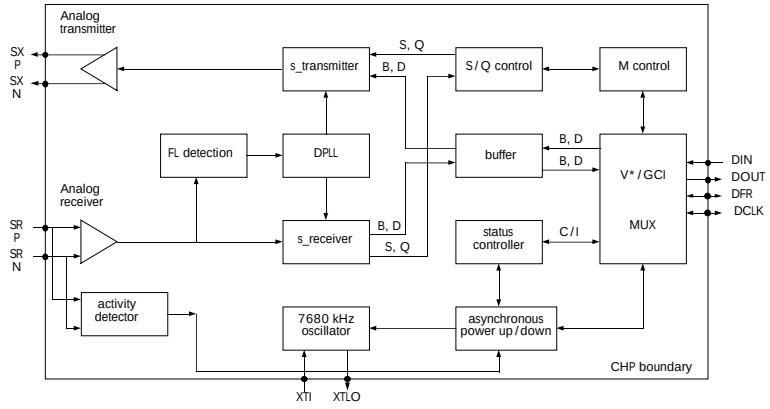


Fig. 23 : Block Diagram of the S-interface

GCI Clock Synchronization in the ISDN Environment for the Upstream S-Interface (NT)

In general the downstream devices are slaved to the upstream devices.

The S-interface is master of the S-bus, and can sample the received (upstream) S-bus frames with a receive clock at exactly the transmit frequency, but with an unknown phase.

The S-interface receives the GCI timing, and must derive the 192 kHz S-bus bit-clock from it. As the GCI timing is not necessarily a multiple of 192 kHz, the S-interface generates a 192 kHz TX and RX clock from a clock input at 7680 kHz +/- 100 ppm. The 192 kHz is not a pure divide by 40 of the X-tal, but is locked to the 8 kHz frame signal of the GCI-interface. This is a DPLL action where the 192 kHz clock period can be adjusted 1/40 of the 192 kHz clock period every 250 us. Note that jitter on the 192 kbit S-bus signals is a combination of the jitter on the 7680 kHz before the DPLL and the effects of the DPLL locking to the GCI 8 kHz frame.

The S-bus RX clock in fixed timing (short passive bus) is derived from the same clock input with the same frequency correction as the transmit clock, but with a phase offset. The corrections of 1/40 of a bit period are used in open loop here.

The S-bus RX clock in adaptive timing (extended bus, point to point) is also derived from the same master clock. However, the receiver must optimize the symbol sampling moment. This is an extra phase correction, which tracks wander and jitter of the received data. The receiver tracks the RX data by locking on the F/L transitions.

Note: The timing stays identical for an internal loop from TX to RX, because then the S-interface uses adaptive RX timing as well. Even an external S-bus loop can be applied, provided that the receiver does NOT work with fixed RX timing.

Conclusion: the S-interface block has 3 different clocks, which are locked in frequency, but with unknown phase relation. Because the clocks are derived via DPLL blocks the phase relation is not constant, but has some jitter and wander.

Clock Speed

The master clock runs at 7680 kHz +/- 100 PPM.
Internally the S-bus transceiver part runs at 192 kHz, derived from the master clock, but locked to the ISDN network clock with a phase locked loop, adjusting one 7.68 MHz period every 250 us. The ISDN network clock is sent downstream via the S-bus or the GCI interface.
The GCI part runs at the clockspeed of its interface, which is 512 kHz in NT mode.

Power Saving/Deactivation of the S-Interface

The S-interface is controlled via the GCI interface. This interface is designed to be shut down and consequently reactivated. Shutting the bus down is commanded by the controller on the bus. Once the command is acknowledged, there exists a fixed procedure to halt the clock (by the controller in NT). Reactivating the bus can be done by the S-interface or the controller.

When the GCI bus is going to be shut down, the S-bus transceiver is put to idle also. The S-bus transceiver enables an asynchronous signal detector, which can reactivate the S-interface on receipt of INFO via the S-bus. Then the S-interface shuts down the internal 7.68 MHz clock distribution. If the clock is externally provided it can be put to idle also, after the GCI bus has become idle.
The S-interface can receive activation via the S-bus during the process of shutting down via the GCI bus.

Activation of the S-Interface in NT mode

Activation through the S-bus will be seen by the signal detector. The S-interface does not need a GCI clock to activate the GCI interface, which it does by asynchronously pulling the data line low. The master on the bus answers with GCI and frame, followed by commands via the C/I channel. The bus master also delivers the 7.68 MHz frequency simultaneously with GCI activation.

Activation through the GCI bus consists of clock and frame delivery, followed by commands via the C/I channel. The S-interface will activate the S-bus transceiver according to the commands, including the internal clock distribution. If the master clock must be delivered to S-interface. Note that the internal clock distribution to the S-tranceiver section is delayed for 2 ms (using the GCI frame-clock).

Detailed Operational Description of the S-bus Interface

Introduction

In this section, external and internal operational details of the S-bus interface are given. Detailed interface timing and electrical specifications are given in related documents.

General Characteristics

The S-interface realizes full-duplex transmission of two B-channels (64 kbit/s each) and one D-channel (16 kbit/s). Additionally the S-interface allows controlled access to the common D-channel and the activation/ deactivation of each connected device.

Transmission Rate

The nominal transmission rate is 192 kbit/s in each direction. There is no requirement for special bit sequences in the B-channels.

Frame Structure

Data is transmitted within a frame of 48 bits in each direction. The nominal frame period is 250 us which gives a frequency of 4 kHz. The frame structure is not depending on 'bus' or 'point-to-point' configuration.

AMI S-bus Coding

For both directions a pseudo-ternary coding (AMI) is used. A binary '1' (high level logic) is coded as 'no signal' whereas a binary '0' sequence is represented by alternating positive and negative pulses.
The polarity inversions, coupled with a minimal density of marks per frame, reduce the low frequency components of the signal. The 4 kHz frame always starts with a positive pulse (F-bit), followed by a negative balance bit L.
Balance Bits

Inside the frame more balance bits are present serving two purposes:

1) In both directions they guarantee that the polarity of the first bit or F-bit is constant. They also increase the mark density on the link.
2) Moreover, in uplink direction the bits in the frame can be generated by different terminals. Therefore, the frame is subdivided in groups of bits, each sent by a single terminal and terminated also with a balance bit. The first binary '0' of each group of bits except for the framing signal is coded as a negative pulse. The balance L-bit finishes those group with a positive mark if needed, to avoid violations of the mark inversion scheme. This allows the different B and D channel bits to be sent by different transmitters on a bus, because the AMI polarity is always fixed. Thus no AMI violation can be caused by the multipoint nature of the bus.

AMI Violations for Frame Synchronization

For synchronization purposes the AMI is violated twice per frame. A 48 bit frame always starts with a positive pulse (F-bit) followed by a negative balance bit L. The F-bit is a violation, because the last mark of the previous frame is positive also. The first binary '0' following a framing signal (F, L) is always negative, and is a second violation.

Frame Synchronization Distance Rule

There are two AMI violations in the frame: the F-bit at the beginning is at a fixed position. The second violation must follow the F-bit within 13 bit positions, because the frame contains an FA (auxiliary flag) at position 14, which is a binary 0, even if all other bits (2 to 13) are binary one. After the FA the next violation will be the F flag itself, at a distance much larger than13 bit positions. This distance rule allows for fast and reliable frame flag detection.

Frame Synchronization Multiframing Exceptions

AMI violation delay in multiframing:
At the TE/LT-T position the received FA bit is occasionally a binary 1 in case of multiframing. However, then the N bit at position 15 is a binary one, because it is the binary inverse of the FA. This guarantees a second violation within 14 positions after the F-bit.

AMI violation exception in multiframing:
At the NT/LT-S position the received FA bit is occasionally a binary 1 in case of multiframing. FA is followed by a balance bit L, which is then also at binary 1. If all B and D bits between F-L and FA-L are also at binary 1, then there is no second violation within the 14 positions. If the remaining bits (B and D channels) are also at 1 in the remainder of the 48 bit frame, then the second violation will be absent and next F-bit will be no violation! This can delay the synchronization and could trigger an invalid loss of synchronization.
The delayed synchronization during multiframing is unavoidable. To avoid an invalid loss of sync at the NT/LT-S when multiframing is on, all incorrect second violations (too late or missing) in uplink direction are ignored if the FA bit was a binary 1 in the corresponding 48 bit frame in downlink direction. Missing violation at the F-bit position are ignored if the preceeding 48 bit frame (downlink) had the FA-bit at one.

Synchronization Principles - Adaptive Bit Timing

1) The receiver first finds the AMI violations by oversampling.
2) Immediate bit-synchronization is given by the F-L transition.
3) The distance rule of the next violation within 14 positions is used to validate the F-bit.
4) Frame synchronization is acquired after 3 correct frames, with a correct F-bit violation and a second one within 14 bit positions.
5) The F-L transition determines the adaptive bit sampling.
6) At NT/LT-S loss of sync after two frames not having F violation or second violation following the distance rule (at 14 bits), when no multiframing is active. The downlink signal stays active, but changes automatically from INFO4 to INFO2. In case of multiframing we ignore missing second violation within the 14 bit distance, or the missing violation at the next F-bit for uplink frames with the corresponding downlink FA bit at binary 1.

Synchronization Principles - Fixed Bus Timing

On a short passive bus the position of the bit sampling can be fixed.
The points 3), 4) and 6) of the previous paragraph are executed. No oversampling is done, no DPLL action is needed to track the F-L adge.
Note that the fixed timing is changed automatically to adaptive timing, when internal S-bus loops are commanded. When external S-bus loops are used (e.g. for production test) only adaptive timing is suitable!

Pulse Polarity in the S-bus Frame

The receiver is polarity independent. The transmitter in NT mode has no polarity requirements.

Table 18

Signals from network to terminal		Signals from terminal to network	
INFO0	No signal, open circuit	INFO0	No signal, open circuit
INFO2	Frame with all bits of B, D, and E-Echo channels, and A bit at binary zero, FA, M, S, N and L bits follow the coding rules	INFO1	Continuous signal with the following pattern: positive zero, negative ZERO, six ONEs
INFO4	Frame with operational data on B, D, and E-Echo channels. Bit A set to binary ONE. FA, M, S, N, L bits follow to coding	INFO3	Synchronized frames with operational data on B, D channels. FA and L bits according to normal coding
TEST1	Send Single Zeros (SSZ), AMI marks, 250 us distance forced via pin (NT) or C/I	TEST1	Send Single Zeros (SSZ), AMI marks, 250 us distance forced via pin (NT) or C/I
TEST2	Send Continuous Zeros (SCZ), alternating marks, forced via pin (NT) or C/I	TEST2	Send Continuous Zeros (SCZ), alternating marks forced via pin (NT) or C/I

Transmitted Frames

Depending on the activation state of the-interface the S-interface can transmit different signals called INFO 0, 1, 2, 3, and 4. Moreover two testsignals are defined:

The B-channel and D-channel are transparently transmitted on the S-bus. When idle those channels are all binary 1.

Details on Downlink Frames

The downlink frames transmitted by upstream devices contain an E-bit. During INFO4 the E-bit is the echoed D-channel-bit received from the downstream devices. This D-echo-channel is used for D-channel access procedure.

Two L-bits are used for DC-balancing, after the F-bit and the last bit the frame. In downlink direction some special bits are used:
- A-bit used for activation (A=1 for INFO4, A=0 for INFO2);
- S-bit coded as binary zero, if no multiframing active;
- N-bit coded as N = .NOT. FA (applies to INFO2 and INFO4);
- M-bit at binary zero, except when multiframing;
- FA-bit, additional flag (bin. zero), except when multiframing.

Without multiframing active S, FA, M bits are binary zeros. Multiframing is allowed to be active during INFO2 and INFO4 and influences the S, FA, M bits.

Details on Uplink Frames

The INFO3 frame transmitted at terminal-side consists of several groups of bits, each of them DC-balanced by an adjacent symmetry bit L.
The uplink D-channel requires an access protocol. Downlink multiframing influences the FA-bit in uplink (Q-channel):
If the S-interface receives the FA-bit as binary 0 (electrical mark) it will always answer with binary 0.
If the S-interface sees the FA-bit as binary 1 it answers with binary 1, when multiframing is not active.

S-bus Transmitter Timing and Framing

The transmitter data are sent at 192 kHz. The 192 kHz are derived from the master frequency of 7.68 MHz, by division by 40. The transmitter framing is at 4 kHz. The timing is slaved to the downlink clocks, the 4 kHz S-bus frame is locked in phase to the available downlink framing.

Transmitter Timing and Framing at the NT

With a DPLL the 192 kHz is locked to the GCI interface, by synchronizing the S-bus frame with the GCI frame. The DPLL locks the falling edge of the F/L frame signal on the GCI frame signal. Jitter is according to the CCITT I.430 spec.

S-bus Reciever Timing and Synchronization

RX Frame Sync and Bit Sampling in NT Short Passive Bus Mode

The bit-sampling moment is fixed, and coupled with the TX bit clock, which is derived from the master clock, and locked to the GCI frame. The RX bit counters (counting the position of the uplink bits in the frame) are also locked to the downlink/TX bit counter. Uplink data are 2 counts late.

The fixed bit sampling moment is advanced 5 periods of the 7.68 MHz clock, before the edges of the S-interface transmit data stream. This is needed to allow an advance of 7% or 3 periods of the uplink data, allowed according to the CCITT to be sent by TE at zero distance, combined with a 1 period jump of the downlink data clock derived from the master clock.

This relationship is valid on the S-bus itself. Inside the S-interface the actual bit sampling must be delayed to account for the nominal delay of the external transformer, the internal filters and driver delays. The total delay of the external devices was estimated at 100 ns, the internal delay is implementation related. Moreover, the sampling can be delayed extra by 5 periods of the 7.68 MHz clock via the XTR4 pin, and also via internal register programming.

The frame synchronization knows the F position, and applies the rules explained earlier (i.e. without over- sampling). The NT in fixed bus mode can be forced to loop the S-bus signals internally! Then S-interface applies adaptive timing, to test a maximal functionality.

Frame Synchronization Details in Adaptive Timing

During synchronization the device oversamples the incoming bits with a fixed threshold, which is at 33 % of the nominal pulse height, with AGC active.

First Violation Detection

The oversampling is done at the 7.68 Mhz master clock, or at a factor 40. A simple voting technique is used to detect a violation: the detector output increments a counter as long as the detected bits are marks of the same polarity or zeros. When a polarity change of the marks is seen, the counter is cleared. Whenever a sequence of more than 50 oversampled marks of the same polarity are seen, the receiver decides that a violation came in. The number 50 must not be too large, to allow synchronization on signals with flat edges.

After finding a single violation, the oversampling looks for the mark-to-zero and the subsequent zero-to- opposite-mark transition which it uses to estimate the actual F/L crossing; see next paragraph.

Violation Validation

During the hunt for frame synchronization the F/L transition forces the RX bit sampling clock and bit counter in an deterministic state, which is optimal. The RX part now hunts for a next violation. In fact the next mark must be a violation. This violation (polarity should be opposite, but this is ignored) must arrive before the counter indicates 14 received bits. If the second violation is found before 14 received bits, the F/L must be validated for 2 more consecutive frames. In all following frames the F/L transition is oversampled to lock the RX bit sampling clocks with DPLL movements of 1 period of 7.68 MHz. If the F/L validation is not correct during the 2 subsequent frames, the S-interface restarts its hunt.

RX Bit Synchronization NT Adaptive Bus

Bit synchronization is done only by detection of the F-L zero crossing. This is optimal for short busses and extended busses, where multiple signal sources are present, each with an independent bit timing. Only the F/L is a "stable" combination of all electrical drivers on the bus. For long point to point links the same technique is used, although averaging of all zero crossings would be better, theoretically.

Each time the bit counters indicate the reception of F/L, the RX part oversamples the transition at 7.68 MHz.

The F/L crossing is used for several purposes:

1) It gives an immediate estimate of the RX data optimal sampling moment, after a first violation is found, via oversampling.
2) It indicates how to correct the RX 192 kHz sampling clock each frame by one 7.68 MHz period (DPLL action in adaptive RX sampling).

The "F-L zero crossing" is not detected. The S-interface detects the transition mark-zero (instant t1) and the subsequent zero-opposite-mark (instant t2). During the F/L bits the device oversamples the incoming signal with a fixed threshold, which is ALWAYS at 33 % of the nominal pulse height.

In between t1 and t2 the RX part counts "Y", the number of zeros, ignoring possible marks. The zero count Y is less than the t2-t1, because noise could force marks to be seen by the receiver during the interval.

The number "Y" of intermediate zeros is used to estimate the slope of the arriving signal, to predict the edge of the F/L transition. Y is limited to 15, which corresponds to a first order time constant of 2 us for the S-bus data, filtered by the S-interface input filter. This is 2.5 times slower than the worst case point to point signal as specified in CCITT I.430.

Note that Y could be larger than 15 if the zero crossing is sought on a mark which is followed by a zero bit, i.e. when the violation is not the F bit followed by L.

Immediate Bit Synchronization at Instant t2

When the receiver is not synchronized the receiver is oversampling and hunts for violations.
The F/L crossing is found at instant t2 and the 192 kHz bit clock is preset to predict an optimal sampling moment. The data edge is estimated at instant (t2 - 2.00*Y).
The optimal sampling precedes the theoretical edge by 8 periods of the 7.68 MHz clock. The advance is needed to allow a jitter of +/- 7% (15% or 6 periods of 7.68 MHz) of the data, allowed according to the CCITT to be sent by any TE, combined with a 1 period DPLL correction needed at the NT to correct for its own X-tal.

Continuous Bit Synchronization at Each F/L Crossing

Once the receiver is synchronized on the data, the F/L edge is used on each frame to validate the sampling moment. The oversampling clock is used in the F/L window to validate the zero crossing.

At instant t2 (zero to opposite mark transition) the state of the counter generating the 192 kHz clock from the 7.68 MHz is compared with the optimal value, which should be loaded for an immediate bit synchronization as explained above. If the difference (in # of periods of 7.68 MHz) is -1, 0, or 1, the counter is not changed, to provide hysteresis. If the difference is larger, the counters are adjusted with only 1 1/40, to limit the DPLL reaction.

In this manner the sampling moment is adjusted with one 7.68 MHz period, every 250 us. At the TE this allows a maximal frequency error of the X-tal of 500 PPM.

Timing Relation Between RX and TX on the S-bus in NT Mode

The delay between transmitted and received frames at NT is 2 bits plus the roundtrip delay across the S-interface, in normal operation. Worst case delay between downlink frames and uplink frames is 42 us (see CCITT) or 8 bits. Longer delays cause problems to correctly send the E-channel bits. In loopback mode, the delay is zero.

The receiver in NT is conceived to accept any delay, while in adaptive sampling mode. This is convenient when looping the S-bus signals. E-channel operation is only correct if the delay is 0 to 8 bits.
The delay trimming via XTR4 or X4 pin delays the sampling moment with 5 periods of the 7.68 Mhz clock or 650 ns in NT mode with fixed timing on short bus. In the adaptive timing mode no effect is seen.

The delay trimming can also be controlled via the GCI M-channel adding another 650 ns to the effect of the XTR4 pin.

Frame Relation Between GCI and S-Interface

If the S-interface is in the Network position, the 192 kHz S-bus bit clock is derived from the master clock, which is locked to the 8 kHz frame of the GCI bus.
The leading edge of the F-bit starts the frame on the S-bus. The DPLL forces this F-bit edge in a fixed range relative to the frame signal of the GCI bus.
The F-bit start is situated in a 520 ns zone starting with the edge beween bit0 and bit1 on the GCI bus. The uncertainty is caused by the DPLL actions which will correct the 192 kHz S-bus clock in steps of 130 ns, i.e. one 7.68 MHz period.
This phase relation optimizes the total roundtrip delay on the S-bus for each B-channel, if the GCI clock is 512 kHz.
The delay of the NT with S-bus looped is only 125 us for both B-channels at the GCI side.

E-Channel Generation

At the NT site the S-interfaceA mirrors the uplink D-bits in the downlink E-channel. The purpose of the E-channel is to control the D-channel access from multiple TEs on the S-bus.
In INFO2 the E-bits are zero, in INFO4 the E-channel mirrors the preceding D-channel bit received in the S-bus receiver.

Multiframing - S and Q Channels

The S-interface block supports multiframing according to I.430 but multiframing is disabled on chip.

S-Interface Programming

M-Channel Messages and Registers

In the INTQ, the S-interface block can operate in its normal mode, or can be selected to operate in a reduced function mode compatible with earlier devices.

Introduction

In the S-interface block, the M-Channel is used for the transfer of operation and maintenance information:

1) The TRANSFER of system related registers (S and Q channel of multitraming);
2) The WRITE and READ operations of internal registers;
   - Test and identification registers;
   - Mode registers, overriding the default state, changing the modes without having to change straps;
   - Control registers to change auxilliary inputs and outputs;
   - Status registers, e.g. alarm and error monitoring;
3) The transfer of the BUSY indication for the D-channel access, present in all modes.
   In the reduced mode, the use of the M-channel is not necessary. However, it is available to access the multiframe S and Q bits, and to access some internal registers with added features.

M-Channel Receiver and Transmitter

In the S-interface the M-channel tranceiver works half-duplex, with messages lenght 2 bytes, with the M-channel going to idle after every message, to allow a change of direction in the S-interface M-transceiver.

General Content of M-Channel Messages

In the S-interface block, the M-channel messages are limited to double bytes. The first nybble of the message is a general address, defined in the GCI standards. In the S-interface this address nibble is limited to:

0001b, used to access S and Q channel bits;
1000b, used to read or write internal registers.

All other values are ignored.

S and Q Channel Messages

This feature is disabled on the INTQ.

Internal Register M-Channel Messages

All internal register operations on the M-channel are double byte messages. Both READ and WRITE operations are possible. After every operation, the M-channel must go idle again. Concatenation of double byte messages could result in errors. Messages which are aborted are ignored. The S-interface block debounces the different bytes of the message.
A WRITE operation is a one way message, acknowledged only via the MR bit. However, every register can be read. A READ operation results in an answer, delivering the CONTENT. The READ operation causes the two directions of the M-channel to be logically dependent! After the READ message to the S-interface block the incoming M-channel must return to IDLE. The M-transceiver in the S-interface block gives priority to the delivery of the CONTENT and/or S/Q messages, before it can handle the next incoming READ/WRITE or S/Q message.

M-Channel Operations

M-Channel Format - Bit and Byte Numbering Convention

The M-channel is a byte oriented channel. Bytes (also called octets) are transmitted in ascending numerical order. Within a byte the most significant bit is transmitted first. The four most significant bits of the first message byte represent a general address, discussed under 7.3.

Byte Transfer Procedure

To transfer a message composed of subsequent bytes on the GCI M-channel each byte is presented by the transmitter and acknowledged by the receiver. For that purpose the two M-channels (to and from the S-interface) have separate handshake bits, the MR and MX bits in the B1*-channel. The MX bit signals the presence of new information in the M-byte, the MR bit signals the reading of the information by the receiver.

Idle M-Channel

The procedure starts from idle, where MX and MR are both inactive at 1. The M-channel content during idle is invalid and should be at FFh. However, the idle value received by the S-interface is ignored.

Start of Message (SOM) and First Byte Transfer

From the idle state a start of message transmission is initiated by the sender with the transition of the MX-bit from inactive to the active state. The data to be transmitted are passed in the M-byte starting in the same frame as the MX-bit activation. In normal operation the first byte must be kept constant in the M-channel until the SOM is acknowledged by the receiver.

Acknowledge of the SOM and First Byte

On detection of the SOM the receiver will read the M-byte. It will acknowledge reception, provided that identical data were seen in the M-channel during two consecutive frames. To acknowledge SOM and the first byte, the MR bit goes from inactive to the active state, remaining there, until:

1) a next byte is transferred, with MX indication, see next paragraph;
2) an EOM is signalled by the transmitter;
3) the receiver wants to abort the message.

Further Byte Transfers

In the case of the second byte transfer, the sender must detect the transition of the MR bit of the receiver from inactive to the active state (negative edge 1 to 0), before transmitting the second byte, see previous paragraph. The sender indicates a new byte of information by the transition of the MX bit from active to inactive, for exactly one frame. The data is valid in the same frame. The next frame the MX bit goes from inactive to active, and the valid data are repeated. The data are thus repeated for minimally two frames. The sender repeats the data in all subsequent frames until the receiver returns the MR bit inactive, to acknowledge the data (see next paragraph), or to abort the message.

Further Byte Acknowledgement

Each subsequent byte (signaled by MX going high for one frame, see previous paragraph) is acknowledged by the receiver once it has seen two consecutive identical bytes in the M-channel. It acknowledges it by putting the MR inactive (at 1) for exactly one frame. In the next frame the MR bit must go back to active.

End of Message (EOM)

Once the sender has received the acknowledge of the last byte, it changes the content to FFh, moves the MX to inactive and keeps it inactive for at least two frames.

Acknowledge of EOM

After the EOM of the sender, the receiver acknowledges the EOM by putting MR bit in the inactive state for at least two frames, keeping it there until the transmitter goes active again.

Sender Not Ready

If the sender is not ready (second byte or subsequent) the MX bit will be kept in the active state and the channel byte stays constant.

Receiver Not Ready

If the receiver is not ready for the first byte it keeps the MR in the inactive state. If the receiver is not ready for the second byte, it refuses to acknowledge the bytes by keeping MR in the active state.

IDLE Forced From Sender

If the first byte is never acknowledged, i.e. MR staying at 1, the sender can force the M-channel and MX to IDLE. If the reception of a subsequent byte is not (or not yet) acknowledged (MR is staying active at 0) by the receiver, the sender can put the M-channel and MX to IDLE. The receiver should return MR to inactive. The last byte or even the complete message are never really acknowledged by the receiver.

Abort Request From Receiver

The receiver can abort a message after the SOM acknowledge or any subsequent byte acknowledge by forcing MR inactive for at least two frames. The S-interface aborts a message only when it is forced in hard reset.

Acknowledge Abort

The sender acknowledges the abort request by entering the idle state.

Reset of the M-Channel Transceiver

At reset, the M-channel transceiver is forced to the idle state.
All message bytes are put to idle, the MX and MR bits are forced to 1, aborting any ongoing message.

Write Operation

For a Write operation, the double byte messages is as follows:

Table 19

To S i/f block	byte 1:	1	0	0	0	X	ADR2	ADR1	ADRO
	byte 2:	CONTENT (MSB first to LSB last)							

There is no outgoing message in reaction to the WRITE.
The second nibble is address of the internal register, limited from 1 to 6 in the S-interface block. The write addresses must differ from 0000, otherwise the READ operation is assumed.

Read Operation and Content

For a READ operation, the double byte messages is as follows:

Table 20

To S i/f block	byte 1:	1	0	0	0	0	0	0	0
	byte 2:	X	X	X	X	X	ADR2	ADR1	ADRO

The second nibble is all zero for an internal READ operation. The fourth nibble is the address of the register,

The answer is the CONTENT message, two bytes as follows:

From S i/f block	byte 1:	1	0	0	0	BUSY	ADR2	ADR1	ADRO
	byte 2:	CONTENT (MSB first to LSB last)							

The second nibble is the address of the internal register. The second byte contains the content of the register. The BUSY kit, when set, indicates that the D Channel is in use.

Detailed Bitmap of the Internal Registers

Table 21

Address	name	sent first			Bits				sent last	Access
0h	ID	0	1	1	0	BUSY	0	0	0	read
1h	VN	0	0	0	0	BUSY	X	X	X	read
2h	CONF	BT1/SC	BTO	DEX1	DEXO	BUSY	MFE	LTS/T	DELT	rd/wr
3h	OUT	AUX4b 1	AUX4b 0	AUX3b 1	AUX3b 0	BUSY	TEST	AUX1 b 1	AUX1 b 0	rd/wr
4h	IN1	AUX4	AUX3	-	AUX1	BUSY	MOD2	MOD1	MOD0	read
5h	IN2	(TEST)	SCLK	XTR4	XTR3	BUSY	XTR2	XTR1	XTR0	read
6h	PERF	S1/Qb1	S1/Qb2	S1/QB3	S1/Qb4	BUSY	SLIP	MFR	BER	read
7h	TEST	device test only; not used in normal operation								rd/wr

Identification Register Read Only Address 0h

Table 22

ID	0	1	1	0	BUSY	0	0	0

Version Number Register Read and Write Address 1h

Table 23

VN	0	0	0	0	BUSY	X	X	X

The version number of the device starts at 00h.

Configuration Register Read and Write Address 2h

Table 24

CONF	BT1/SC	BT0	DEX1	DEX0	BUSY	MFE	RES	DELT
reset	0	0	0	0	0	0	0	0

BT1/SC	BT0	bus type selection
0	X	bus type according to BUS pin; value at reset;
1	0	bus type = Adaptive; BUS pin ignored, pin usable as I/O;
1	1	bus type = Fixed; BUS pin ignored.

DEX1	DEX0	Common Echo Bus mode selection
0	X	No operation.
1	0	DE/CEB bus not active.
1	1	DE/CEB bus driven and sensed.

BUSY	READ only bit. Must be writen at 0, writing BUSY at 1 triggers testmodes.
MFE	Multiframing enable if 1; Reset value is 0. Always write as 0. Multiframing is disabled in the MTC-20276.
RES	Not used in this configuration. Always write 0. (Reserved)
DELT	Delay triming: compensate 650 ns on the fixed bus sampling in the NT, transceiver roundtrip. Setting this bit increases the delay to 1300ns.

Output Register Read and Write Address 3h

Table 25

OUT	RES4b1	RES4b0	RES3b1	RES3b0	BUSY	TEST	RES1 b1	RES1 b0
reset	0	0	0	0	0	0	0	0

Note: The RES(i) pins are reserved and cannot be used in this configuration.

BUSY	Read only bit. Must be written 0, writing BUSY 1 triggers test modes.
TEST	Must be written 0, writing TEST 1 triggers test modes.

IN1 and IN2 Registers Read Only Addresses 4h and 5h

Table 26

IN1 Reads	AUX4 x	1 1	AUX3 x	AUX1 1	BUSY BUSY	MOD2 1	MOD1 reduced mode select	MODO 1
IN2 Reads	(TEST)	SCLK 1	XTR4 DELT	XTR3 S-bus mode	BUSY BUSY	XTR2 TSP	XTR1 0	XTR0 0

The bits represent the binary level of the input pin. All values are sampled asynchronously at the moment the content message is assembled. The BUSY bit is also present here.

Performance Register Read Only Address 6h

Table 27

PERF	RES	RES	RES	RES	BUSY	RES	MFR	BER

The RES bits are reserved and cannot be used in this configuration.

RES	Always reads as 0
MFR	Indicates Multiframing synchronization if at 1.
BER	Set each time the BER signal goes low, reset after being read.

BER : Bit Error Rate. This indicate that the SIC blocks has seen excessive bit errors, indicating a link transmission problem.

M-Channel operation messages overview

Table 28

register name	to the SIC block				from the SIC block	
	read messsage		write message		content message	
	byte 1	byte 2	byte 1	byte 2	byte 1	byte 2
identification	80h	00h	-	-	80h	content
version number	80h	01h	-	-	81h	content
configuration	80h	02h	82h	content	82h	content
output	80h	03h	83h	content	83h	content
input1	80h	04h	(test only)		84h	content
input2	80h	05h	(test only)		85h	content
performance	80h	06h	-_	-	86h	content
test	(test only)		(test only)		(test only)	
S/Q channel	-	-	1Fh	S/Q	1Fh	S/Q

Package Specification

Device Branding

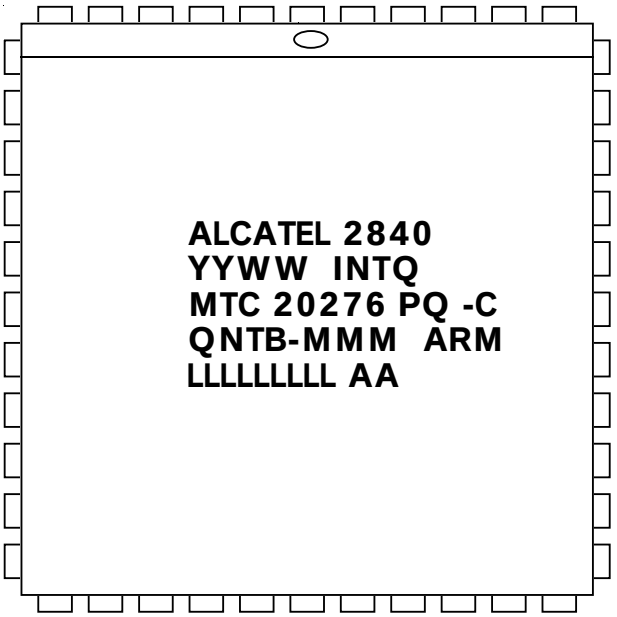


Fig.24c: Device Marking-PC **Order number MTC-20276 PC-I or C**

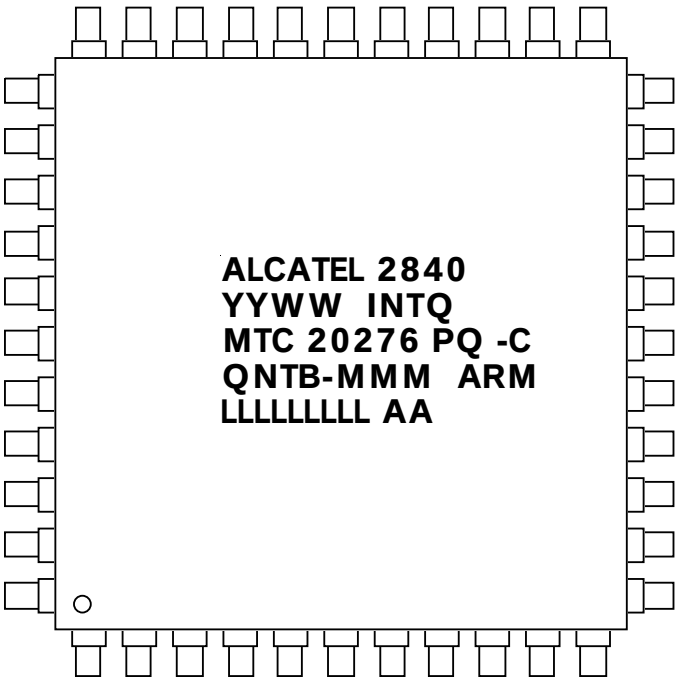
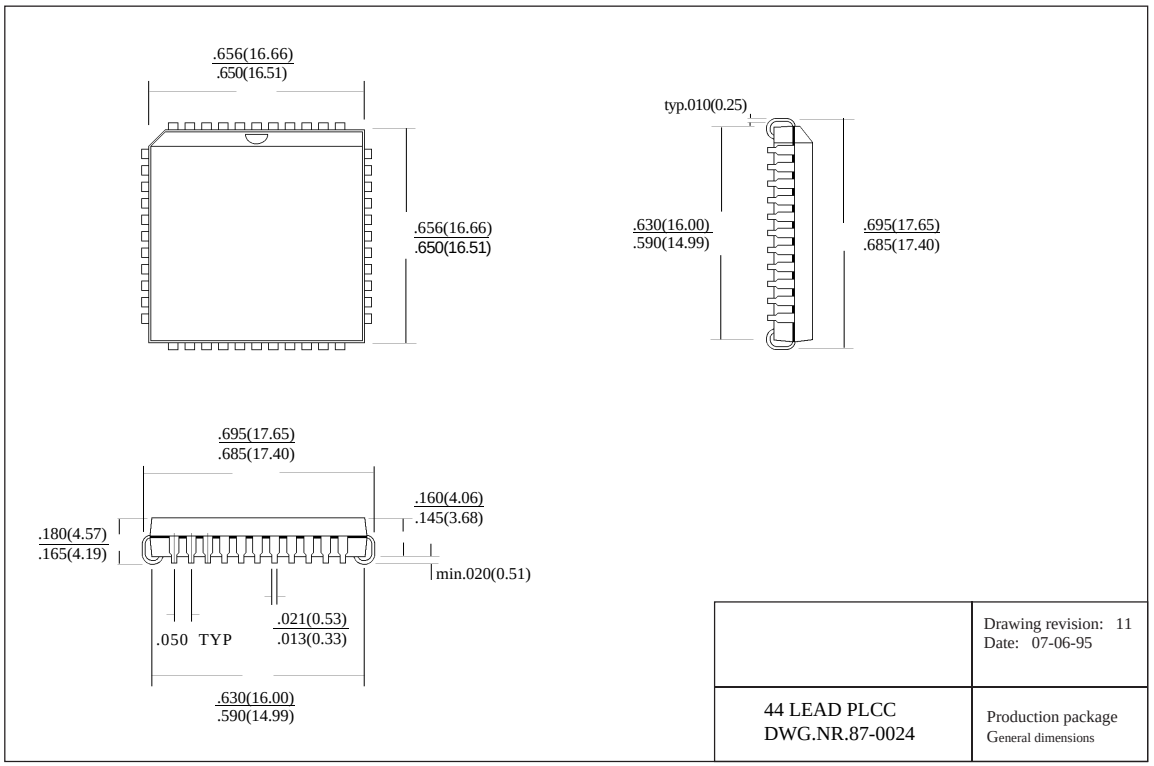
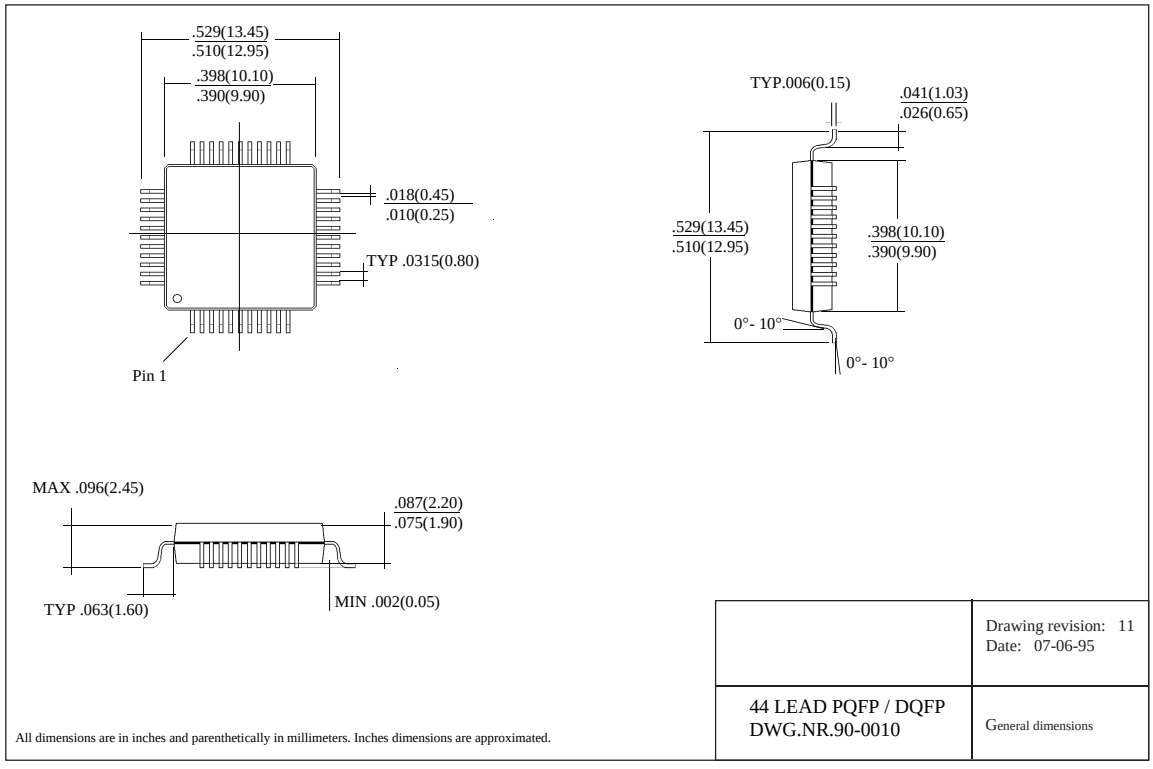


Fig.24d: Device Marking-PQ **Order number MTC-20276 PQ-I or C**

44PQFP and 44PLCC Mechanical Specification



	Drawing revision: 11 Date: 07-06-95
44 LEAD PLCC DWG.NR.87-0024	Production package General dimensions



	Drawing revision: 11 Date: 07-06-95
44 LEAD PQFP / DQFP DWG.NR.90-0010	General dimensions

All dimensions are in inches and parenthetically in millimeters. Inches dimensions are approximated.

MTC-20276 INTQ Compliance Issues Compatibility with ETSI/ANSI Specs

This application note discusses the functional implementation of certain system features which are either optional or not clearly defined in the prevailing international standards ETSI ETR80 (Sept. 95) and ANSI T1.601-1990. The points discussed here are applicable to mask revision QNTB-NAB.

EOC Data Channel

This is not implemented. The ETSI ETR80 (Sept. 95) and ANSI T1.601-1990 mention this data channel, but do not describe how it should be used.

NTM Bit Is Not Supported (SET to 1)

This is an optional feature of ETSI ETR80

AIB Bit Is Ignored

This is an optional feature of ETSI ETR80

After U-only Activation, the Loopbacks (2B+D, B1, B2) Are Not Transparent.

This is a logical consequence of the fact that only the U is activated. However, ETSI ETR80 does not describe the characteristics of the loopbacks in U-only activation (and in normal activation, the loopbacks should be transparent).

The Event 'UOA=0 and DEA=1' in State NT6(a) and NT6 Triggers Transition to NT8(A) (ETR80)

ETSI ETR80 specifies as next state 'NT8(a) or NT8(c)'. The MTC-20276 uses NT8(a).

New INFO1 Received

ETSI ETR80 is ambiguous (in NOTE 12, p. 84) : It states "when INFO1 remains continuously after the NT fails to bring up the network side and returns to state NT1, the NT does not go again into state NT2 unless a new transition from INFO0 to INFO1 is received".
Two interpretations are possible :
1. 'success' is INFO3 reception instead of INFO1 (i.e. arrival into state NT7).
2. 'success' is arrival into state 'active' (NT8).
The MTC-20276 uses the first interpretation.

TL : Tolerance on Recognised 10khz

The tolerance is not clear in ETSI ETR80. Currently, 8.6khz and 11.7khz are used as specified pass/fail points (i.e. a factor of 1.36 between these 2 frequencies, as in the implementation of 4B3T in the MTC-20277 INTT device).

Autoact

Reset of the chip (or power-up) automatically causes an activation (as in ETSI ETR80, ANSI - clause 6.4, ANSI. Table C.1).

ACT-bit (NT->LT) During 2B+D Loopback

There is a difference between ETSI ETR80-1995 and ANSI T1.601 for the 2B+D loopback case :
- act bit (NT->LT) :
ANSI: always 0
ETSI: 0 until synchronised on its own transmitted INFO2, then 1
- start of upstream transparency :
ANSI: on receipt of 2B+D loopback request
ETSI: on receipt of 'act-bit = 1' from LT.
The ETSI approach is chosen, as ANSI is in the process of aligning itself to ETSI (the contribution has been voted on the ANSI T1E1.4 living list).

S/T Only Activation

This feature is described in ANSI92, in Section C.5. It occurs when the NT does not acquire the superframe marker within 15s. This feature appears to be optional, but is not stated as such. It appears not to be present in ETSI ETR80, and to cause different behaviour from the ETR80 activation tables (i.e. the actions on event '15s expired' in states 3, 4, 5) and in the ANSI tables C.1 and C.4. Currently, it is not implemented.

EOC Message Notification of Corrupted CRC : Impact on FEBE_from_NT ?

ETSI ETR80. ANSI T1.601 do not describe an NT- action that should be the consequence of the above EOC message. One could argue that the FEBE bit sent by the NT should then be fixed to 0 or 1. However, we currently keep the definition of FEBE that reflects the comparison between the NT-computed CRC and the CRC received in the frame (as is the case when the CRC is not corrupted).

ANSI NT Maintenance Modes

Metallic Loop Terminator for North American applications only. (ANSI Section 6.5)

Loss of Signal in State NT5

ETSI ETR80 and ANSI specify 'no action', when the signal is lost in state NT5. This means that the system does not deactivate until the 15s timer M4 is expired. The implementation is as described in ETR80/ANSI.

Response to EOC-message 'Notification of Corrupted CRC'

ETSI ETR80 and ANSI do not explicitly state what the NT has to send back. The INTQ sends back 'unable to comply'.

Time Between end EC-training and Going into Power-down

ETSI ETR80 specifies this time as 480ms. The current MTC-20276 implementation uses 960ms, to allow a test system to respond more slowly than 480ms.

MTC-20276 INTQ

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