- emitter-/source-di/dt-feedback (see chapter 3.4.1),
- increase of gate voltage during active clamping (see chapter 3.6.3.2).

Overtemperature

Dangerous overtemperatures arise, if the maximum junction temperature indicated by the device manufacturer is exceeded (e.g. T_{jmax} = 150°C for silicon devices).

During inverter operation overtemperatures might be generated by:
- increase of energy dissipation caused by fault currents,
- increase of energy dissipation caused by defective drivers,
- failure of the cooling system.

3.6.2 Behaviour of IGBTs and MOSFETs during overload and short-circuit operation

Overload:

Basically, the switching and on-state behaviour under overload does not distinguish from „standard operation“ under rating conditions. In order not to exceed the maximum junction temperature, the overload range has to be restricted, since increased load current will cause increased power dissipation in the device.
In this respect limits are set by the absolute value of the junction temperature as well as by overload temperature cycles.
These limits are indicated in the datasheet SOA-diagrams.
Figure 3.52 shows selected examples for MOSFETs and IGBTs.

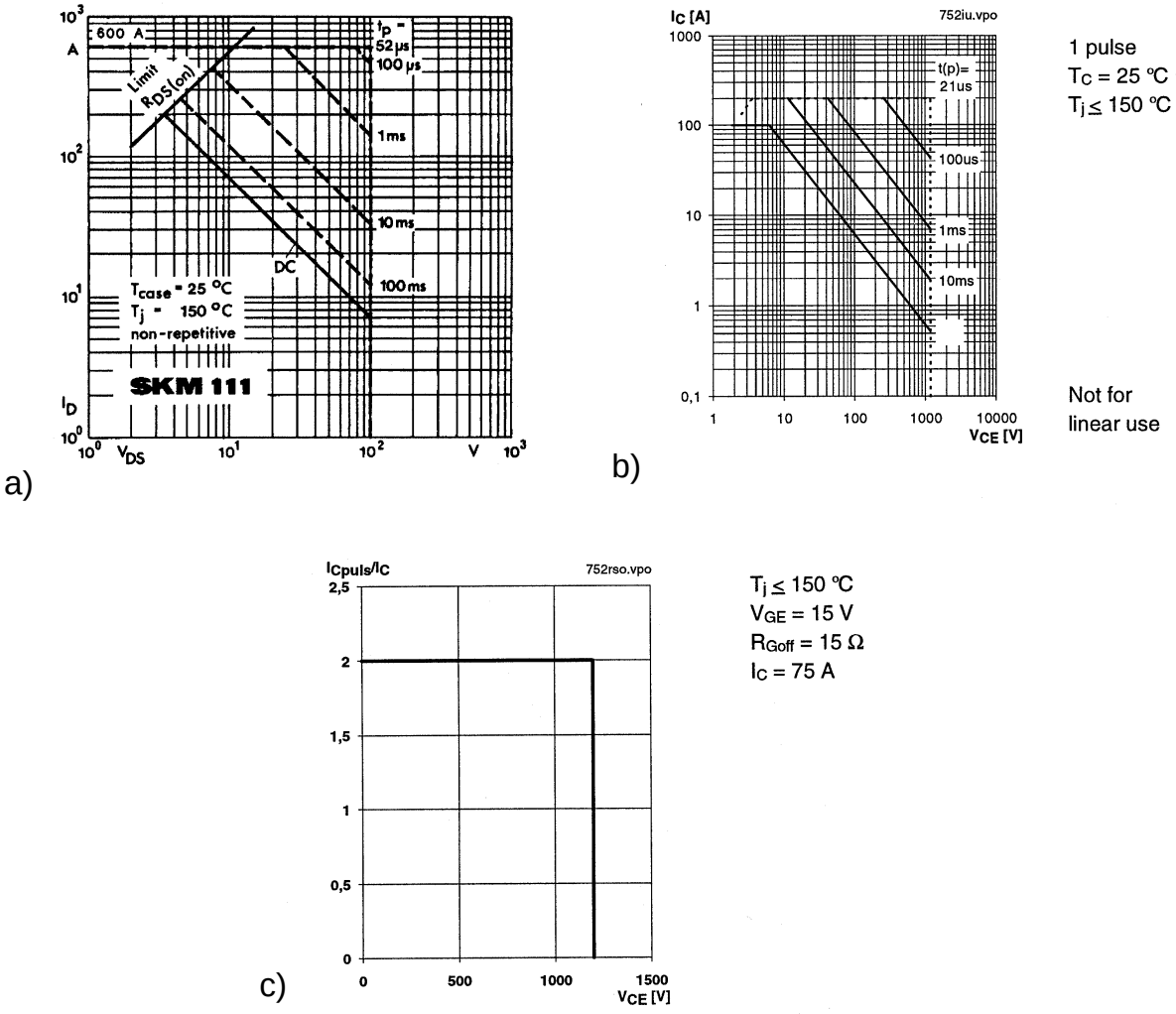


Figure 3.52 SOA-diagrams for MOSFETs and IGBTs
a) Max. safe operating area MOSFET SKM111
b) Max. safe operating area IGBT SKM100GB123D
c) Turn-off safe operating area (! periodic !) IGBT SKM100GB123D

Short circuit:

Principally, IGBTs and MOSFETs are short-circuit proof, i.e. they may be subjected to short circuits under certain given conditions and turn them off, without damaging the power semiconductors.

When considering short circuits (which is to be done with IGBTs), two different cases of short circuits have to be distinguish.

Short circuit I (SC I)

In case of SC I the transistor is turned on to an existing load short circuit, i.e. full DC-link voltage is applied to the transistor already before the short circuit occurs. The di/dt of the short-circuit current is determined by the driver parameters (driver voltage, gate resistor). This transistor current increase will induce a voltage drop over the parasitic inductance of the short circuit, which is depicted as a decrease of the collector-emitter voltage characteristic (Figure 3.53).

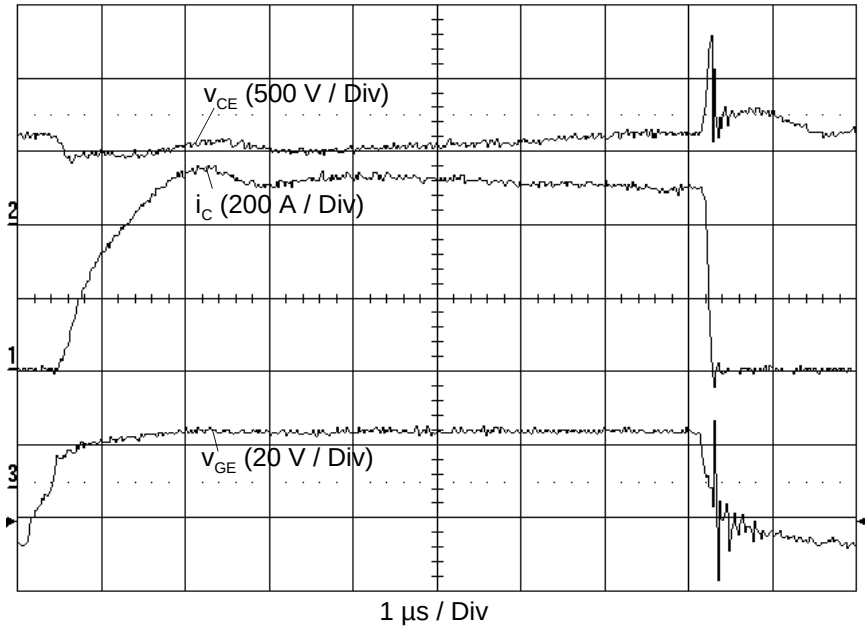


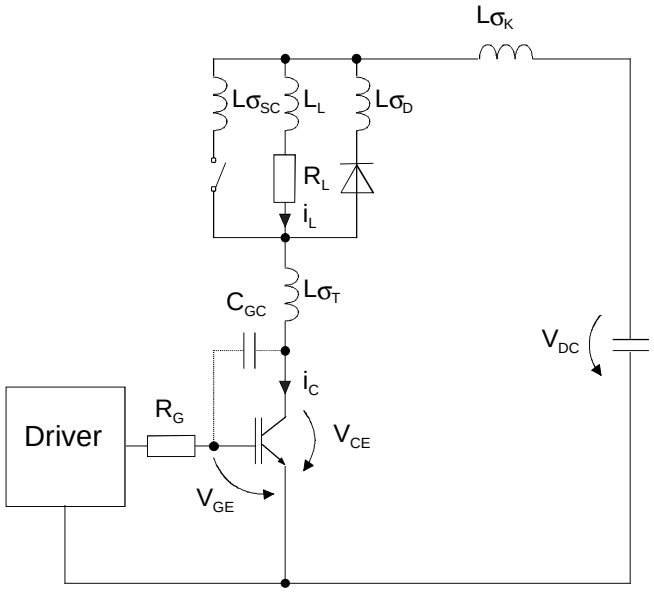
Figure 3.53 SC I characteristics of an IGBT (SKM100GB123D)

The stationary short-circuit current adjusts itself to a value that is determined by the output characteristic of the transistor. Typical values for IGBTs are up to 8-10 fold rated current (see Figure 3.56b).

Short circuit II (SC II)

In this case the transistor is already turned on, before the short circuit occurs. Compared to SC I, this case is much more critical with respect to transistor stress.

Figure 3.54 shows an equivalent circuit and principle characteristics to explain the SC II process.



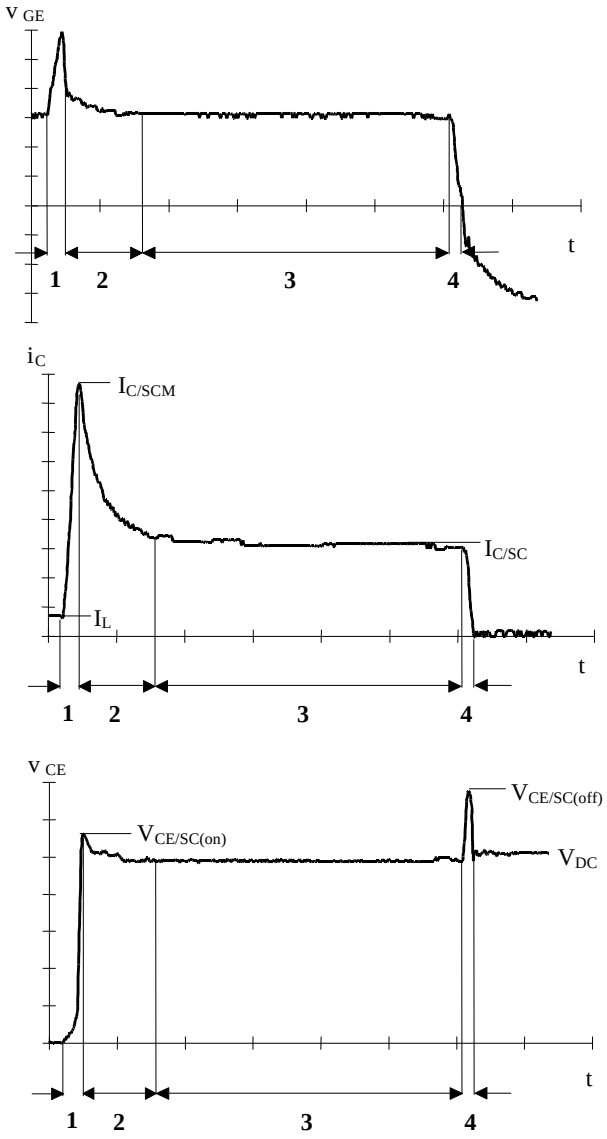


Figure 3.54 Equivalent circuit and principle characteristics of SC II [194]

As soon as the short circuit has occurred, the collector current will increase very steeply, the di/dt is determined by DC-link voltage V_{DC} and the inductance of the short-circuit loop.

During time interval 1 the IGBT is desaturated. The consequently high dv/dt of the collector-emitter voltage will effect a displacement current through the gate-collector capacitance, which increases the gate-emitter voltage. This in turn will cause a dynamic short-circuit peak current $I_{C/SCM}$.

After having completed the desaturation phase, the short-circuit current will drop to its static value $I_{C/SC}$ (time interval 2). During this procedure, a voltage will be induced over the parasitic inductances, which becomes effective as overvoltage in the IGBT.

The stationary short-circuit phase (time interval 3) is followed by turn-off of the short-circuit current towards the commutation circuit inductance L_K, which will again induce an overvoltage to the IGBT (time interval 4).

The transistor overvoltages induced during a short circuit may exceed the values of normal operation by several times.

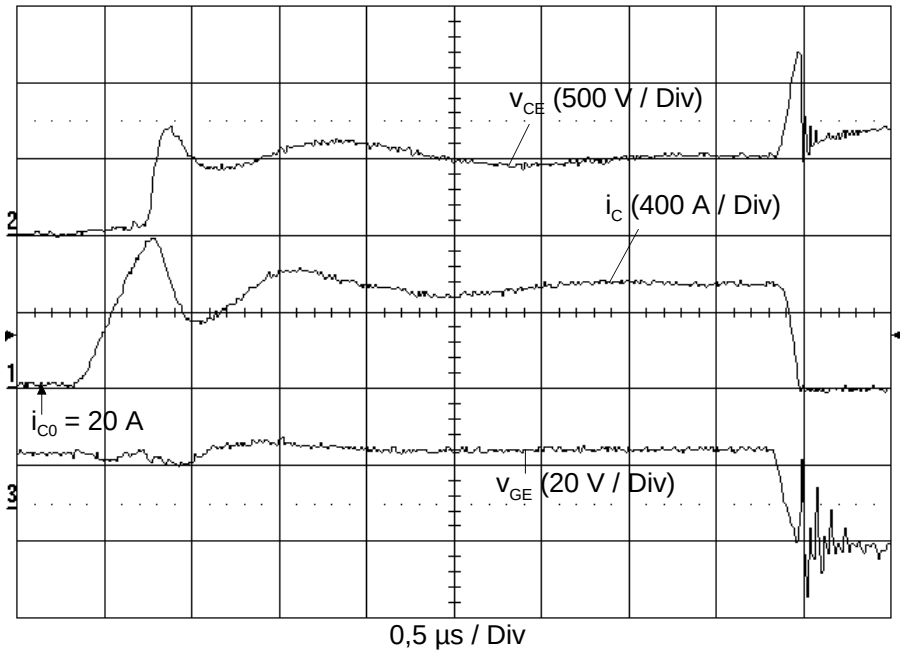
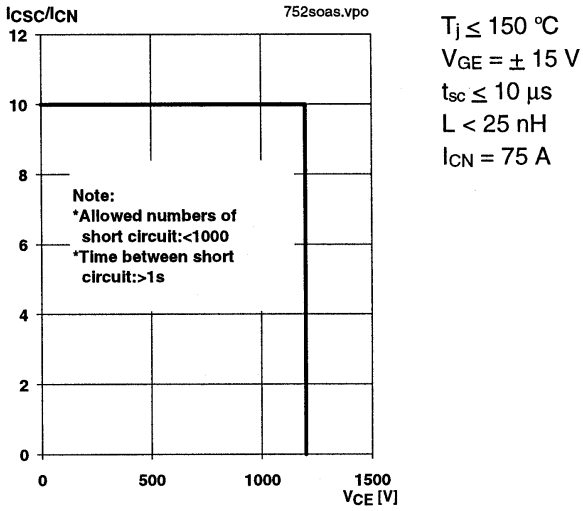


Figure 3.55 SC II characteristics of an IGBT (SKM100GB123D with gate clamping)

The SOA-diagram at short circuit shown in the IGBT datasheets shows the limits for safe control of a short circuit (Figure 3.56a).

a)



b)

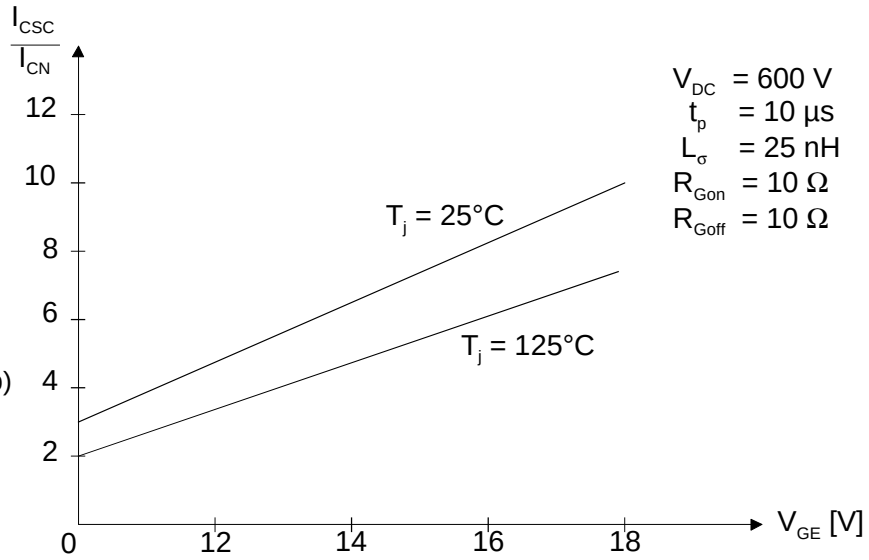


Figure 3.56 SOA at short circuit of an NPT-IGBT (SC SOA)
a) Normalized short-circuit current versus collector-emitter voltage (SKM100GB123D)
b) Normalized short-circuit current versus gate-emitter voltage (general)

The following important boundary conditions have to be fulfilled to guarantee safe operation:
- the short circuit has to be detected and turned off within max. 10 µs,
- the time between two short circuits has to be at least 1 second,
- the IGBT must not be subjected to more than 1000 short circuits during its total operation time.

Figure 3.56b shows the influence of gate-emitter voltage and junction temperature on the stationary short-circuit current.
Short circuit I and II will cause high power dissipations in the transistor, which will increase the junction temperature. Here, the positive temperature coefficient of the collector-emitter voltage has a favourable effect (this also goes for the drain-source voltage), since it causes reduction of the collector current during stationary short circuit (see Figure 3.56b).

Possibilities for reliable detection of fault currents and limitation of occurring overvoltages are summarized in chapter 3.6.3.